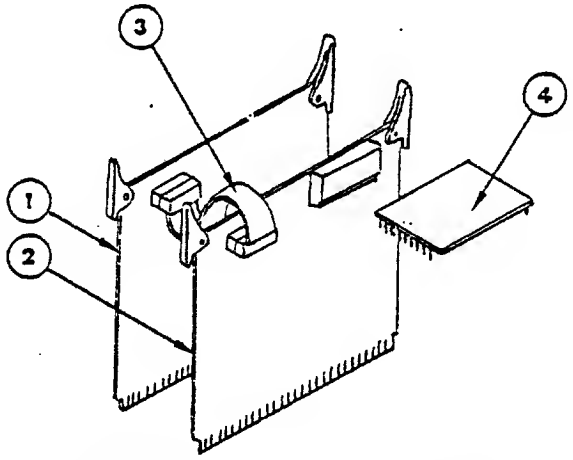
DATA I/O
CORPORATION

INSTRUCTION MANUAL

PROM PROGRAMMER
Program Card Set
909-1183-1

025-1183-1
REV G DEC 77

SPECIFICATION



1.	Digital Card	701-1173
2.	Analog Card	701-1183-1
3.	Interconnect Cable	709-1608
4.	Calib. Program Adapter	910-1183-1

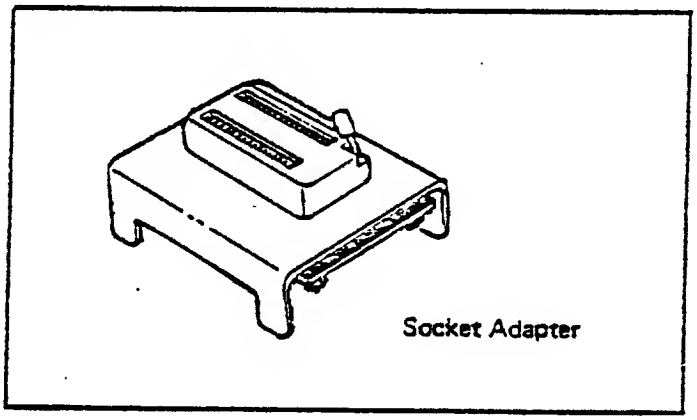
Figure 1-1. Program Card Set 909-1183-1

Table 1-1. PROM types to Data I/O Socket Adapters

Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
ADVANCED MICRO DEVICES				
256x8 MOS	1702/AM9702	VOL TS	24 PIN	1047
256x8 MOS	1702A/AM9702A	VOH TS	24 PIN	1047
INTEL				
256x8 MOS	1702A/4702A/ 8702A	VOH TS	24 PIN	1047
MITSUBISHI				
256x8 MOS	58563 (1702A)	VOH TS	24 PIN	1047
MOSTEK				
256x8 MOS	3702	VOH TS	24 PIN	1047
NATIONAL SEMICONDUCTOR				
256x8 MOS	1702A	VOH TS	24 PIN	1047

DESCRIPTION

Program (Personality) Card Set 909-1183-1, with the appropriate Socket Adapter, provides Data I/O PROM programmers with the capability of programming and reading the PROMs listed in Table 1-1. Socket Adapters are available for each PROM listed. Table 1-1 references the Socket Adapters required to program (or read) the various PROMs.



CALIBRATOR PROGRAM ADAPTOR

Program Card Set 909-1183-1 includes Calibrator Program Adapter 910-1183-1, which mates with the Data I/O Universal Calibrator. As shipped, this Program Card Set is precalibrated according to Data I/O Calibration Procedure 017-1183-1, which is included in the Performance Check Section of this manual.

INSTALLATION

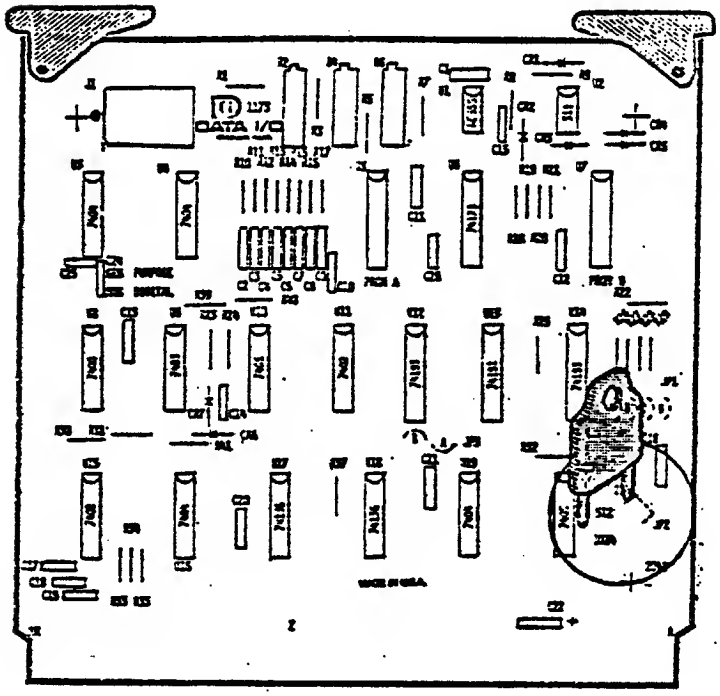
Turn Power OFF while changing Card Sets. Install the Digital Card in programmer Brown-Orange card slot; install the interconnected Analog Card in White-White card slot. Component sides of cards should face forward in programmer Models 1-5, to the right in programmer satellites, and down in programmer Models 7 and 9. Connect J2 on Analog Card to front panel Socket Receptacle. Refer to the programmer manual for more detailed installation instructions.

CALIBRATION AND PERFORMANCE CHECK

Card Set calibration and performance verification procedures are given in the following pages. Calibration should be performed every 90 days, or if PROM programming yields fall below PROM manufacturers' recommendations. Performance Check should be performed after each calibration.

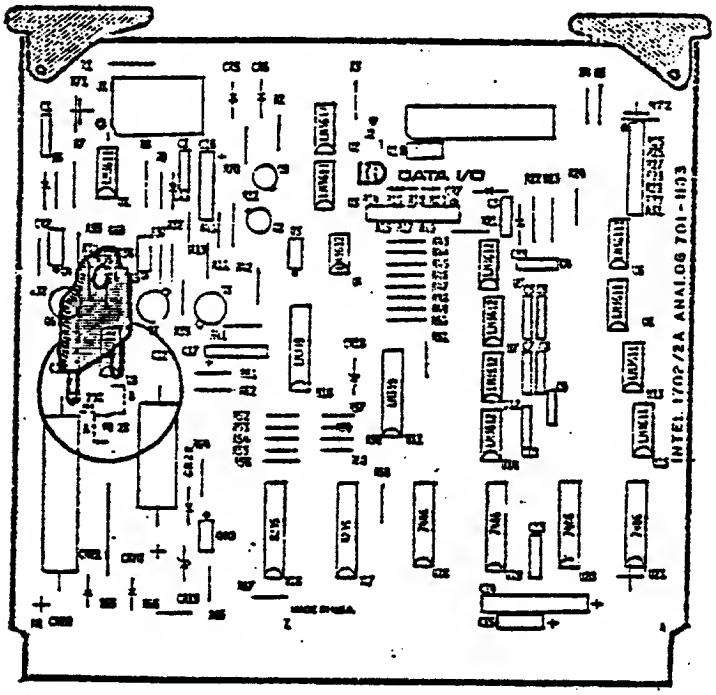
Brown

Orange



White

White



JUMPER POSITIONS

Word Limit Jumper JP10 is located on the lower-right corner of the digital card. This jumper should be in the position marked "256" while programming 1702 and 1702A PROMs.

Duty Cycle Jumper JP1, located on the left side of the analog card, determines program waveform duty cycles. 1702 PROMs are programmed with JP1 in position "A" (2% duty cycle); 1702A PROMs are programmed with JP1 in position "B" (20% duty cycle).

SHORT AND REVERSE DETECTION

If a PROM is plugged in backwards or if it contains an internal short, program card set 909-1183-1 automatically signals a reset and causes the programmer to enter the STOP mode.

INTELLIGENT PROGRAMMING

The number (n) of program pulses applied to a PROM word is a function of the number of pulses required to program the word (x) times a multiplier A, according to the equation,

$$n = x + A(x+1) - 1$$

On the 909-1183-1 program card set A is set at 4 by JP1 on the digital card.

REJECT LEVEL

If a PROM does not program after 256 pulses (set by digital card JP3) reject is signaled, the verify A and B lights extinguish, and the programming and interrupt lights stay on.

CALIBRATION/PERFORMANCE CHECK

INTRODUCTION

Since PROM manufacturers' shipments can vary from lot to lot, slight variations in PROM programming yields are to be expected. However, each manufacturer usually specifies certain minimum PROM programming yields—provided that specific approved programming techniques are employed. Data I/O Programmers employ manufacturer-approved programming techniques: therefore, if programming yields diminish below PROM manufacturers' recommended minimums, or, if the program card set has been in use for more than ninety days since its last calibration, programmer performance should be checked as explained in this section.

The performance check includes calibration adjustments of program waveform amplitudes and includes go/no-go tests of all critical programming parameters. Also included in the performance check are tests on resistively loaded ac waveforms.

DATA I/O FIELD SERVICES

Data I/O, Inc. furnishes complete programmer repair and calibration services at regional Field Service Centers and at the Data I/O factory. Contact your local Data I/O representative for further information.

TEST EQUIPMENT REQUIRED

To perform a complete performance check, the following equipment is required:

1. Data I/O Universal Calibrator, P/N 910-1071.

2. A. Prog. 1, 2, 3, 5: Data I/O Extender Card, P/N 910-1136.
   B. Prog. 9: Data I/O Extender Fixture, P/N 910-1074.

3. Digital Voltmeter: Fluke Model 8000A, or equivalent

4. Adjustment Tool: A three-inch screwdriver

5. Dual Trace Oscilloscope: Tektronix 465, or equivalent

6. Programmers 1, 2, 3, 5 only: Data I/O 13 inch Interconnect Cable, P/N 709-1613.

7. Programmer 9 only: Data I/O Interconnect Cables, P/N 709-1613 and 709-2608.

8. Jumper wires approximately 12 inches in length.

INSTALLATION OF UNIVERSAL CALIBRATOR

The following installation procedure assumes that the Universal Calibrator is mated with the Extender Card and that programmer power is off. On Programmers 1, 2, 3, and 5, remove the top cover to expose the card cage. To expose the card cage on the Model 9, open the access opening on the front of the chassis.

1. Remove end of 26-conductor cable from analog card. Remove both cards (analog and digital) from Programmer (or Satellite) card cage.

2. Remove end of 16 conductor cable from digital card J1.

CAUTION

Connector pins are fragile; careless connector extraction may result in bent or broken pins. Use a suitable tool—like a small screwdriver—when removing connectors from their sockets.

3. Install the extender card (with the Universal Calibrator in place).
   A. Programmers 1-5: Install the extender card into the analog card slot (white-white).
   B. Programmer 9: Install extender fixture into digital card slot (brown- orange).

4. A. Programmers 1-5: Install the analog card of the program card set into the card slot on top of the extender board. Refer to Figure 1.
   B. Programmer Model 9: Install the analog card in front card slot. Refer to Figure 2. The components should face the Calibrator.

5. A. Programmers 1-5: Install the digital card in the digital slot in the programmer.
   B. Programmer 9: Install the digital card behind the analog card on top of the extender card.

6. Making sure that cable red stripes and connector pins 1 are properly oriented, connect the analog card to the Universal Calibrator as follows:
   A. Programmers 1-5: Connect J1 of the analog card to J1 of the Universal Calibrator using the strap between the analog and digital cards. Connect J2 of the analog card to J2 of the Universal Calibrator using the ribbon cable that connects the card set and the programmer.
   B. Programmer 9: Connect J1 of the analog card to J1 of the Universal Calibrator using the strap between the analog and digital cards. Using the 26-connector cable supplied with the Calibrator, connect J2 of the analog card to J2 of the Calibrator.

7. Plug Calibrator Program Adapter into PROGRAM ADAPTER SOCKET on Universal Calibrator.

CAUTION

Be sure that the four-digit portions of both part numbers are identical: i.e. Analog card 701-XXXX is part of program card set 909-XXXX, which is calibrated by calibrator program adapter 910-XXXX.

8. Connect DVM ground probe to GND test point at left side of Universal Calibrator.

This completes installation of the Universal Calibrator.

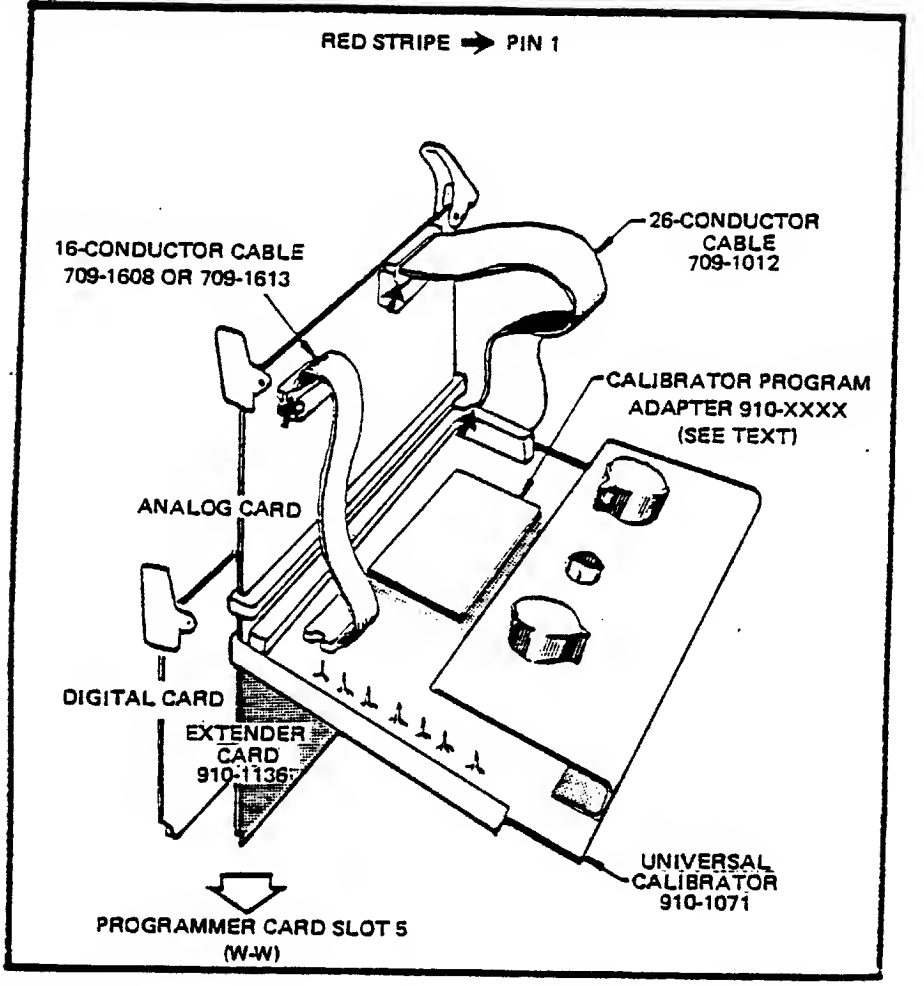


Figure 1. Installation of Universal Calibrator into Programmer Models 1, 2, 3, and 5 for Calibration/Performance Check.

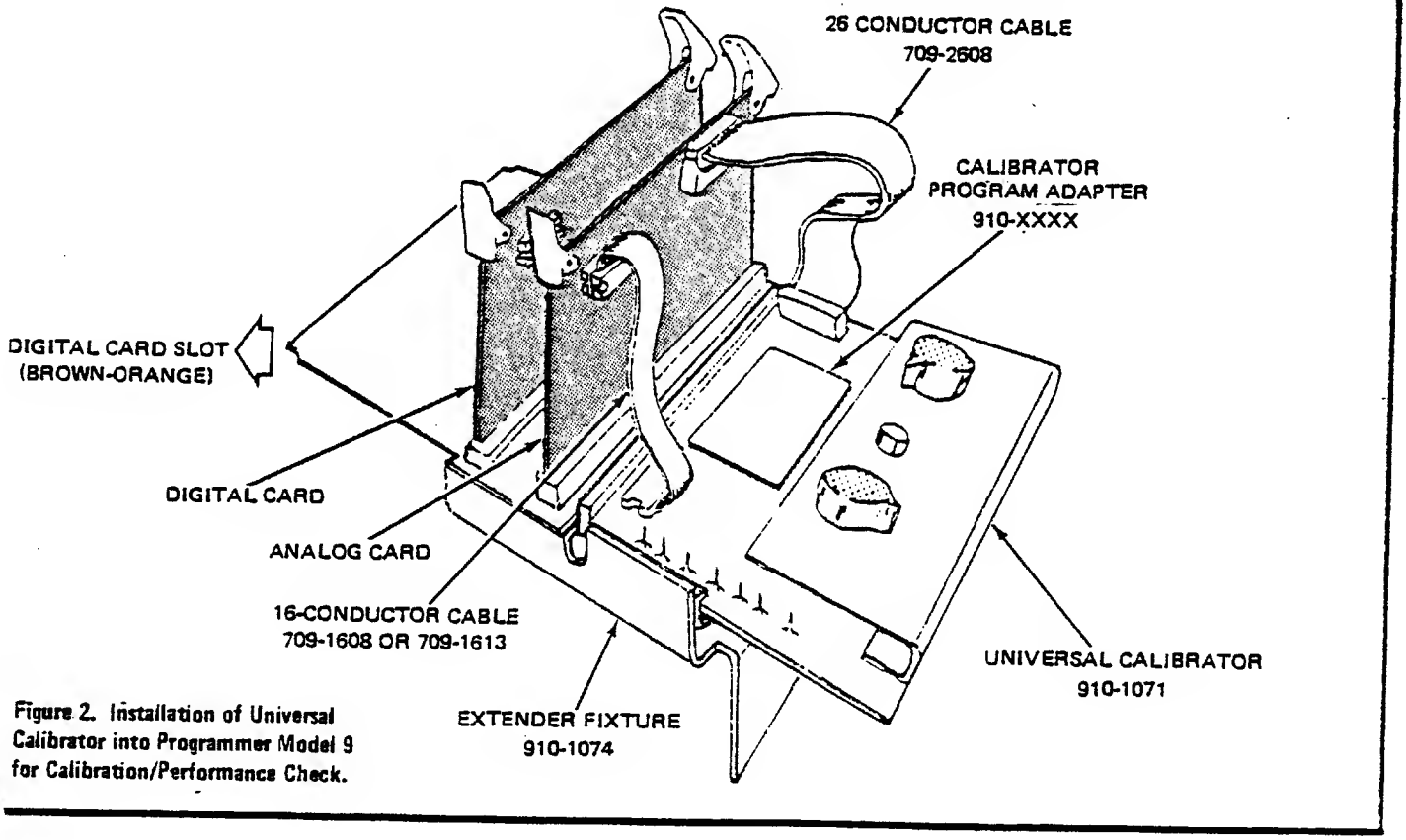


Figure 2. Installation of Universal Calibrator into Programmer Model 9 for Calibration/Performance Check.

CALIBRATION CHART

The calibration chart is to be used only with the (calibrator) program adapter specified in the title block of the chart.

The left-most portion of the chart contains truth tables for the calibrator program adapter. The truth tables are for documentation purposes only, and have no bearing on the actual performance check/calibration procedures.

PROGRAMMER WORD COUNT COLUMN is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When using the chart, refer to the address (word count) corresponding to the address readout configuration of the programmer in use. For instance, if your programmer has a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static (DC steady state) conditions created by the Universal Calibrator may cause thermal damage to compo-components if Programmer is left unattended with advanced word count.

TEST DESCRIPTION column contains three kinds of tests: (1) power supplies, (2) performance checks, and (3) calibration adjustments. The power supply tests are contained in the first five rows of the chart. (Note that power supply adjustments are located in the programmer, not in the program card set.) Performance checks fill the bulk of the Calibration Chart; these are characterized by min/max voltage limits only. No nominal (NOM) values are given, and no adjustments (ADJ) are prescribed.

Calibration steps are those with entries in the ADJ and NOM columns. These steps are evident by the note "CALI-BRATION STEP" in the comments column.

SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load select switch; S3 is the line select switch. Generally, each step on the Calibration Chart requires changing of switch positions. S1 is push to test, and should be held depressed only long enough to obtain a DVM reading.

CAUTION

DO NOT hold S1 depressed for extended periods. Certain measurements induce high Programmer current levels. Extended high current operation (S1 depressed) may damage sensitive electronic components.

TEST POINT column gives test point location for DVM probe on Universal Calibrator. Some test points are located on the program card itself; for instance, if a test point is designated as U6 P8, it means that the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the comments column.

The ADJ column calls out potientiometer designations. The first four entries in the ADJ column refer to power supply potientiometers located on the power supply board of the Programmer. If adjustments are required, refer to Programmer manual. The remaining entries in the ADJ column refer to pots on the analog card. These are located as shown on page 1-2 in the Specifications section of this manual.

The LIMITS COLUMN is divided into three portions: MIN (minimum), NOM (Nominal), and MAX (Maximum). The values given are in volts, and indicate the range into which a given DVM reading should fall when S1 is pressed. If a reading is within the limits, no adjustment is required and the programmer (or program card set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (calibration steps), the card is non functional and should not be used for programming.

NOTES are written in a block at the bottom of the calibration chart. These apply to certain calibration steps and are referenced by numbers in the comments column. Notes called out by letter in the comments column apply only to Model IX calibration.

PERFORMANCE CHECK AND CALIBRATION PROCEDURE

DC CALIBRATION

The following paragraphs describe the method by which a program card set is checked/calibrated in conjunction with the applicable Calibration Chart. The procedure assumes that the Universal Calibrator is properly installed, as previously described. The following procedure should be performed with the programmer in an ambient temperature range between 15°C to 35°C.

Initialization

1. Switch Programmer power ON; allow Programmer to warm up for approximately five minutes.
2. Programmers 1, 2, 3, and 5:
   Press: RESET
   ROM2-ROM2
   MANUAL
   PROGRAM
   START

   Programmer 9:
   Press: EXECUTE
   Set NORMAL/INVERT switch to INVERT.

Power Supply

During the procedure the programmer card cage should contain all boards normally used.

Connect DVM between GND and the Universal Calibrator test points given in Steps 1-1 through 1-5 on the Calibration Chart. Measured voltages should fall within the given limits. (Calibrator Switch positions do not matter.)

If any power supply voltage measurement reading is outside of the given range, adjustment must be made. Power supply adjustments are located on the power supply board within the Programmer.

If a Programmer Satellite is being used, check/calibrate Satellite power supply as explained in Satellite Manual.

Performance Check/Calibration

1. Use FWD and REV keys on Programmer keyboard to index the "address display" (word count) to the decimal (DEC), hexadecimal (HEX), or octal (OCT) address given in the word count column of the calibration chart.

CAUTION

DO NOT leave Word Count advanced beyond 000 for extended periods. Static (DC steady state) conditions created by the Universal Calibrator may cause thermal damage to components if Programmer is left unattended with advanced word count. Press Reset to relieve possible thermal stresses.

2. With Word Count set, and DVM probes installed between GND and the indicated test point on the universal calibrator, set switches S2 and S3 to the positions indicated. Press S1 to test.

CAUTION

DO NOT hold S1 depressed for extended periods. Certain measurements induce high current levels within the Programmer. Extended high current operation (S1 depressed) puts unnecessary stress on sensitive electronic components.

3. While S1 is held, DVM readings should fall between the indicated limits for each measurement. If a DVM reading is outside of limits, or if the reading cannot be adjusted to fall within limits (ADJ column), DO NOT use the card set for programming.

Proceed through the Calibration Chart until all tests have been performed. At the conclusion of testing, turn Programmer power OFF, and proceed to AC Dynamic Tests.

AC CALIBRATION

AC Dynamic Tests

The following procedure is used to obtain the "Program Waveforms" shown on the Timing Diagram at the rear of this manual.

These waveforms, indicated by circled digits (①,②,③,..) on the timing diagram, are identically referenced on the Calibration Chart. The waveforms are obtained by selecting switch positions (S2 and S3) on the Universal Calibrator and feeding the selected signals to an appropriately triggered dual trace oscilloscope.

Test Set-Up

1. Make sure that programmer power is Off.

2. A. Programmers 1-5: Remove the digital card from the card cage. Refer to Figure 3.
   B. Programmer 9: Remove the digital card from the extender. Refer to Figure 4.

3. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.

4. A. Programmers 1-5: Disconnect the other end of the 16-conductor cable from J1 of the analog card. Substitute the 13 inch cable supplied with the Calibrator, and connect J1 of the analog card to J1 of the digital card.
   B. Programmer 9: Connect the free end of the 16-conductor cable to digital card J1, assuring that cable red stripe and connector pin 1 are properly oriented.

5. Connect triggered input channel of dual trace oscilloscope to digital card test pulse. The location of the test pulse on the digital card is noted to the left of the Test waveform on the digital card. Connect the other channel to TP3 on the Calibrator. Re-install the digital card per step 2, above.

6. Using a suitable jumper cable, connect the Read Enable line emanating from analog card J1-16 to ground. (Use either the programmer chassis or the GND test point on the Universal Calibrator.)

7. Programmer 9: Set NORMAL/INVERT switch to INVERT.

CAUTION

Make sure that J1-16 is properly connected to ground. If it is inadvertently connected to any other potential, damage to Programmer components may result.

8. Turn Programmer power ON.

9. Programmers 1, 2, 3, 5:
   Press: RESET
   RAM-RAM
   PROGRAM
   MANUAL
   START
   Programmer 9:
   Press: KEYBOARD

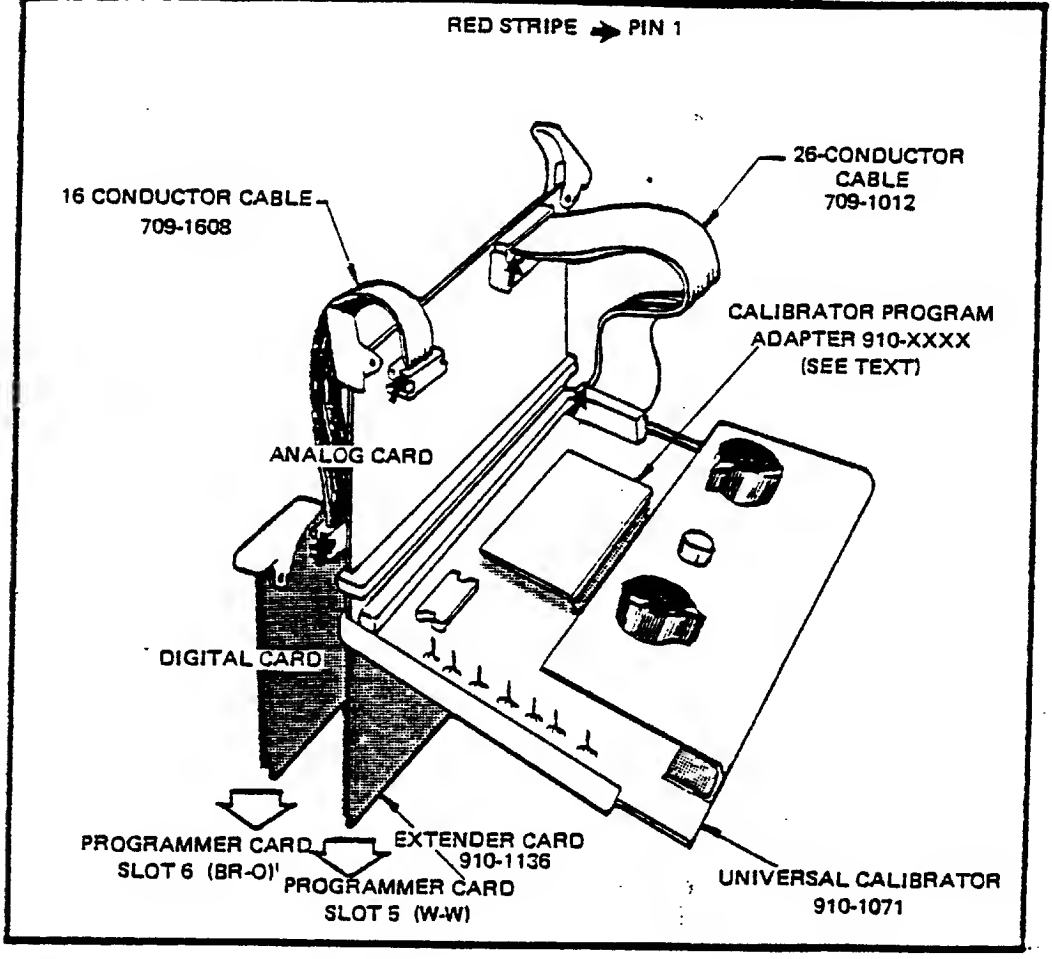


Figure 3. Installation of Universal Calibrator into Programmer Models 1, 2, 3, and 5 for AC Dynamic Tests.

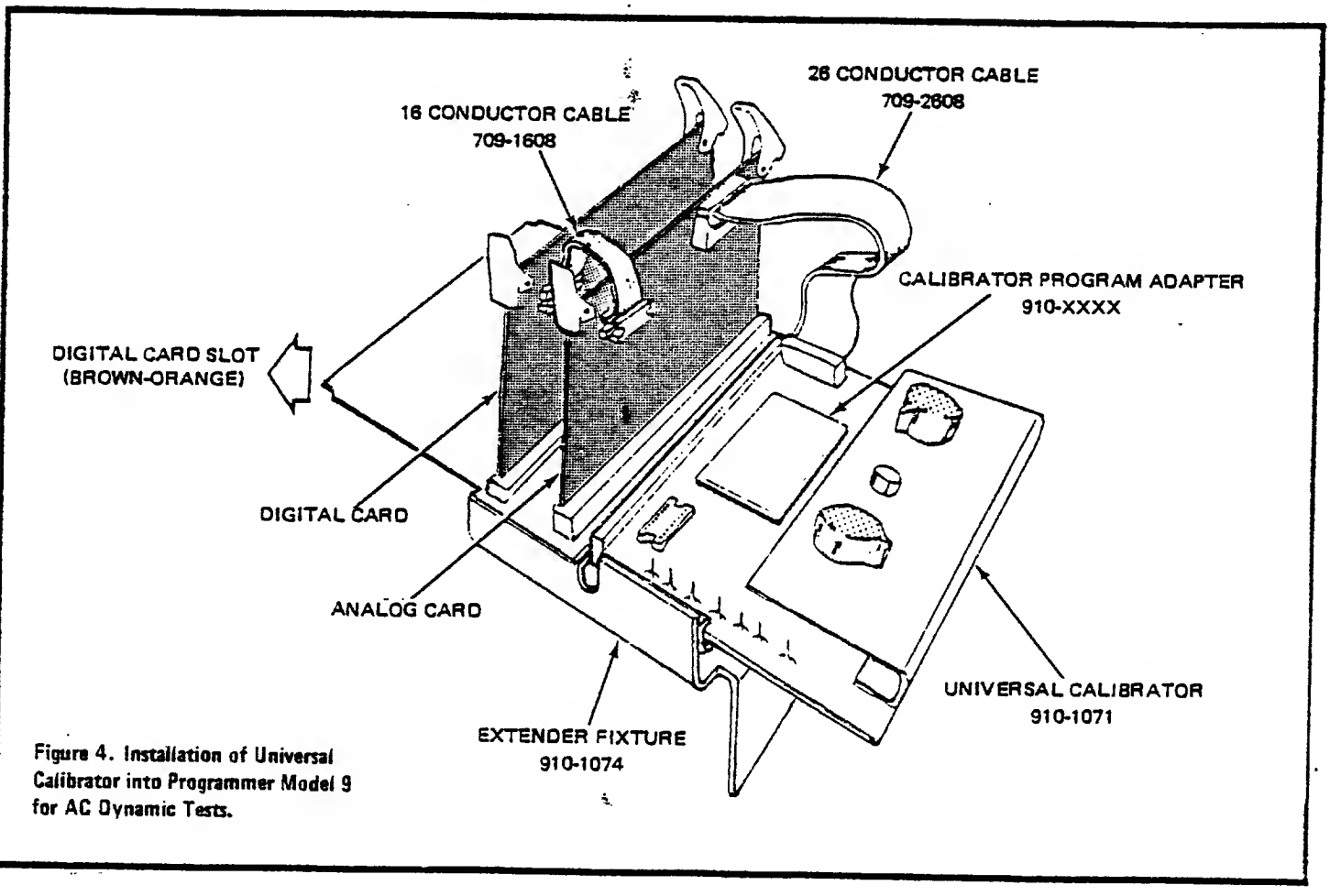


Figure 4. Installation of Universal Calibrator into Programmer Model 9 for AC Dynamic Tests.

10. Load approximately ten RAM addresses with bit 1 (only). This is accomplished by pressing 1 and FWD repetitively, or a tape may be used.

11. Programmers 1, 2, 3, 5:
    Press: RESET
    PROG
    AUTO
    RAM-ROM2

    Programmer 9:
    Press: PROGRAM

Waveform Observations

Initiate waveforms:
Programmers 1-5: press START.
Programmer 9: press EXECUTE.

The machine will stop on those addresses loaded in step 10 of the test set-up. If an abort condition is indicated, press WORD SKIP (SKIP on the Model 9) to advance the word count and repeat output of programming waveforms. An abort condition is indicated on Models 1, 2, 3, and 5 if the PROGRAMMING and INTERRUPT indicators come on. A Model 9 displays an abort condition by flashing the "P" indicator.

The "Program Waveforms" on the timing diagram at the rear of the manual are cross-referenced to the "Test Description" column on the Calibration Chart by circled digits (①, ②, ③, ...). To obtain the various waveforms use S2 and S3 on the Universal Calibrator to select the positions indicated in the "Switch Positions" column of the calibration chart and press S1 to test. S3 routes analog card output to TP3 (oscilloscope probe); S2 selects resistive loads, which are connected to ground when S1 is pressed.

NOTE: *All other information on the calibration charts is of no importance during waveform observations.*

CAUTION

When S1 is pressed high currents are induced within the Programmer; do not hold S1 depressed for extended periods. High currents are also present when the programmer is locked into program mode with advanced word count; RESET before leaving programmer unattended during these tests.

During these tests note that the Abort, Pause, and Reject functions of the program card set remain active; Press WORD SKIP to refresh the display. The abort timer signals a reject after a specific programming time. The pause timer controls the on/off time of the programming function. The position of the reject jumper (C or M) limits the number of applied programming pulses. Refer to the notes column of the timing diagram for definitions of the abort, pause, and reject functions.

6.	Revision "A"	Revision "B" or later
Press:	PROGRAM	EXECUTE
	EXECUTE	Hold SET: press FWD

7. Confirm that the PASS indicator is ON and the programmer is at word count:

	Revision "A"	Revision "B" or later
Press:	1D with the V indicator blinking	1E

Duty Cycle Test

1. Press STOP: press KEYBOARD.
2. Load all bits OFF (Hex ØØ) at address 1D.
3. Advance to word count 1F.
4. Load bit 1 ON (Hex Ø1) at address 1F.
5. Return to address 1F.

6.	Revision "A"	Revision "B" or later
Press:	PROGRAM	EXECUTE
	EXECUTE	Hold SET; press FWD

7. Confirm that the PASS indicator is ON, the programmer is at word count 1F, and P indicator is ON.

Conclusion

This completes the DC tests of the Program Card Set. If PASS is indicated in all three interactive tests, proceed to the Waveform Observation instructions, paragraph 4.4. Replace the analog card and set up calibration equipment as shown in Figure 4-5.

SYSTEM 19

Initialization

1. Turn programmer power OFF.
2. Disconnect the 16-conductor cable (J1) from the analog card and the 26-conductor cable (J2) from the Universal Calibrator.
3. Remove the analog card, with the 26-conductor cable attatched, and set aside.
4. Connect the 16-conductor cable to the digital card J1 with cable red stripe to J1, pin 1. (Other end of cable remains in Calibrator J1.)
5. Refer to the Calibrator Program Adapter installed in the Universal Calibrator. If the circuit board, 702-1073, is Revision "E" or later, install JP1 and JP2 in Position A.
6. Turn Programmer power ON.
7. Press SELECT; key in the Select Code C1, press START.

ABort Test

1. Advance to address 1C: Press KEYBOARD, 1, C and ENTER.
2. Load bit 1 ON (Hex Ø1) to DI bus.
3. Return to address 1C.
4. Press PROGRAM and START.
5. Confirm that the pass indicator on the Calibrator Adapter is ON. The programmer should be at address 1C, and the display should flash.
6. Press KEYBOARD to continue.

INTEractive Test

1. Load all bits OFF (Hex ØØ) at address 1C.
2. Press ENTER.
3. Load bit 1 ON (Hex Ø1) at address 1D.
4. Return to address 1D.
5. Press PROGRAM and START.
6. Confirm that the PASS indicator is ON, with the programmer at address 1E.

Cycle Test ✓

1. Load all bits OFF (Hex ØØ) at address 1D.
2. Advance to address 1F.
3. Load bit 1 ON (Hex Ø1) at address 1F.
4. Return to address 1F.
5. Press PROGRAM and START.
6. Confirm that the PASS indicator is ON, with the programmer at address 1F.

lusion

completes the DC tests of the Program Card Set. If PASS is indicated· ll three interactive tests, proceed to the Waveform Observation instruc- s, paragraph 4.4. Replace the analog card and set up the equipment as n in Figure 4-5.

Calibration Chart

DATA I/O
Programming systems for tomorrow ...today

CALIBRATION CHART 017-1183-1
FIXTURE 702-1071
PROGRAM ADAPTER 910-1183-I
PROGRAM CARD 909-1183-1
MANUFACTURER AMD, INTEL, NATIONAL, MOSTEK
PROM 17D2, 1702A/4702A/8702A AM 97D2

DATE	REV	REVISION RECORD	OR	CK
2-80	D	ECN #3403	EF	VEB
6-6-80	D	ECN #3671	KJB	VEB
2-27-81	D	ECN #4009	EF	DAR
9-25-81	D	ECN #4312	EF	
3-1-82	D	ECN #4492	KB	

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U4	U5	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
07	40	+24	1-1	000	00	000			+24	R26	23.5	24.5	24.5
07	40	Power +48	1-2	000	00	000			+48	R24	49.4	49.7	49.8
07	40	Supply + 5	1-3	000	00	000			+ 5	R18	5.05	5.1	5.15
07	40	- 9	1-4	000	00	000			- 9	R40	-9.2	-9.0	-8.8
07	40	Programmable Supply	1-5	000	00	000			PROGV		14.2		15.2
06	40	VCC Program ①	2-1	001	01	001	2	24	3		47.0		49.0
07	40	VCC Verify	2-3	002	02	002	3	3			13.3		14.7
05	40	V88 Program ②	2-4	003	03	003	2	10			57.8		62.2
07	40	VBB Verify	2-6	004	04	004	3	10			13.3		14.7
07	40	VDD Program	2-7	005	05	005	8	1			0.0		0.4
07	40	VDO Current, IDO Limit	2-8	005	05	005	9	1			0.0		2.0
06	40	VGG Program ④	2-9	006	06	006	7	9			6.0		13.0
47	40	VGG Verify	2-10	007	07	007	7	9			0.0		0.4
27	40	CE Program ③	3-1	008	08	010	7	11			13.3		14.7
07	40	CE Verify	3-2	009	09	011	7	11	✓		0.0		0.3
07	40	Reference Level	4-1	009	09	011	7	U11P8	←		11.5		12.8
07	C0	Bit 8 Program	5-2	010	0A	012	7	23	3		13.3		14.7
07	C0	Bit 7 No Program	5-3	010	0A	012	7	22			0.0		0.3
07	C0	Bit 6 Program	5-4	010	0A	012	7	21			13.3		14.7
07	C0	Bit 5 No Program	5-5	010	0A	012	7	20			0.0		0.3
07	C0	Bit 4 Program	5-6	010	0A	012	7	19			13.3		14.7
07	C0	Bit 3 No Program	5-7	010	0A	012	7	18			0.0		0.3
07	C0	Bit 2 Program	5-8	010	0A	012	7	17			13.3		14.7
07	C0	Bit 1 No Program	5-9	010	0A	012	7	16			0.0		0.3
07	C0	Bit 8 No Program	5-11	010	0A	012	7	23			0.0		0.3
07	C0	Bit 7 Program	5-12	010	0A	012	7	22			13.3		14.7
07	C0	Bit 6 No Program	5-13	010	0A	012	7	21			0.0		0.3
07	C0	Bit 5 Program	5-14	010	0A	012	7	20			13.3		14.7
07	C0	Bit 4 No Program	5-15	010	0A	012	7	19	✓		0.0		0.3

COMMENTS

Switch S1 must be depressed for accurate readings.
CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

Adjustments are located on the power supply board. See programmer manual.

CAUTION: See Note 1.

CAUTION: See Note 1.

Test point located on analog card.

	Model 1-5	9	19	
LOAO	Bits 1,3,5,7 ON	55	AA	DI Bus
Confirm	Bits 2,4,6,8, ON	AA	AA	DO Bus
LOAO	Bits 2,4,6,8, DN	AA	55	OI Bus
Confirm	Bits 1,3,5,7, DN	55	55	OD Bus

DIAGNOSTIC MODEL 19

DATA (LOGIC) LOCATION		TEST DESCRIPTION	STEP NO	WORD COUNT			POSITIONS		TEST PT.	ADJ.	LIMITS		
	U5			DEC	HEX	OCT	S2	S3			MIN	NOM	MAX
07	C0	Bit 3 Program	5-16	010	0A	012	7	18	3		13.3		14.7
07	C0	Bit 2 No Program (7)	5-17	010	0A	012	7	17	3		0.0		0.3
07	C0	Bit 1 Program (6)	5-18	010	0A	012	7	16	3		13.3		14.7
[illegible]	C0	Data Disable	5-20	011	0B	013	7	23	3		13.3		14.7
[illegible]	40	Program Line Program (5)	5-21	012	0C	014	7	12	3		0.0		0.3
17	40	Program Line Verify	5-22	013	0D	015	7	12	3		13.3		14.7
07	C0	Address Test VIL (8)	7-1	170	AA	252	7	15	3		0.0		0.3
07	C0	Address Test VIH	7-2	170	AA	252	7	14	3		13.3		14.7
07	C0	Address Test VIL	7-3	170	AA	252	7	13	3		0.0		0.3
07	C0	Address Test VIH	7-4	170	AA	252	7	4	3		13.3		14.7
07	C0	Address Test VIL	7-5	170	AA	252	7	5	3		0.0		0.3
07	C0	Address Test VIH	7-6	170	AA	252	7	6	3		13.3		14.7
07	C0	Address Test VIL	7-7	170	AA	252	7	7	3		0.0		0.3
07	C0	Address Test VIH	7-8	170	AA	252	7	8	3		13.3		14.7
87	40	Address Test VIH (8)	7-9	172	AC	254	7	15	3		13.3		14.7
83	C0	Address Test VIL	7-10	171	AB	253	7	14	3		0.0		0.3
83	C0	Address Test VIH	7-11	171	AB	253	7	13	3		13.3		14.7
83	C0	Address Test VIL	7-12	171	AB	253	7	4	3		0.0		0.3
83	C0	Address Test VIH	7-13	171	AB	253	7	5	3		13.3		14.7
83	C0	Address Test VIL	7-14	171	AB	253	7	6	3		0.0		0.3
83	C0	Address Test VIL	7-15	171	AB	253	7	7	3		13.3		14.7
83	C0	Address Test VIL	7-16	171	AB	253	7	8	3		0.0		0.3
07	41	Abort Test	8-1	28	1C	034			3				
07	42	Interactive Test	8-2	29	1D	035	For detailed instructions refer to Instruction Manual.						
07	42	Interactive Test	8-3	30	1E	036							
07	07	Duty Cycle Test	8-4	31	1F	037							
07	40	Data Pattern for All Words Not Shown											

	Model 1-5	9	19	
LOAD	Bits 2,4,6,8 ON	AA	55	DI Bus
Confirm	Bits 1,3,5,7,ON	55	55	DO Bus
Confirm	All Bits ON	FF	FF	DO Bus

U3 CAL ADAPTERS	
Words	Data
0-47	B
48-62	9
63	A
64-79	B
80-84	9
85	d
86-91	9
92	A
93-95	9
96-111	B
112	A
113-127	9
128-255	F

Notes: 1. Do not leave Programmer at this word count longer than required to obtain measurement.

NOTES FOR

MODEL IX CALIBRATION

WITH EXISTING SOFTWARE

Note A:

To verify Stop condition, press PROM key, observe output display, should be blank. To resume testing, press Keyboard, then Execute.

Note B:

To observe output buss LED display, press PROM key.

Note C:

To perform "Programmer in FWD," "Programmer in REV" tests, do the following:

a. Ground J1-16 on Analog card
b. Select Load, Execute
c. Press Keyboard, load Hex data 01 for Address 1 only
d. Select Verify, Execute
e. Perform all tests specifying Programmer in FWD
f. Press Skip
g. Perform all tests specifying Programmer in REV
h. To repeat test, select Verify, Execute
i. Remove J1-16 jumper
j. Press Stop, Keyboard, Execute

Note D:

To perform test, press Keyboard; this will pull Stop. To resume testing, press Execute.

Note E:

To perform test:

Clear RAM: Select Invert, press Edit and hold while pressing Load.

a. Press Keyboard, set Address to 000. Load Hex data pattern as called out on calibration chart.
b. Select Program.
c. Ground J1-16 on Analog card
d. Press Execute, wait for programmer to abort; Stop, Keyboard, Execute
e. Release Ground on J1-16
f. Advance to word count specified on calibration chart to make measurement
g. Press PROM for output display, perform measurement
h. Repeat steps a-g for compliment data pattern

Certain MOS Program Card Sets utilize interactive programming techniques. That is, pulse duty cycles are controlled by PROM temperature, and the re-program pulse train lengths are proportional to the number of pulses required to initially program particular PROM words.

Performance check of MOS interactive functions requires installation of the Digital Card into the Universal Calibrator. These tests, if required, are found at the bottom of the Calibration Chart under the heading, "INTERACTIVE PROGRAMMING TESTS," and should be performed following Analog Card tests.

1. Turn programmer power OFF.
2. Unplug connector J1 at the Analog card; unplug connector J2 at the Universal Calibrator.
3. Connect 16-conductor cable to Digital Card J1 with cable red stripe to J1, pin 1. (Other end of cable remains in Calibrator J1.)

Test Procedure:

To test the interactive programming functions of the MOS Digital Card, proceed as follows:

1. Initialization
   a. Turn Programmer power ON.
   b. Press Keyboard
   c. Set Address 01C.
   d. Load Data 01.

2. Abort Test
   a. Press Program
   b. Press Execute
   c. After several seconds, observe PASS indicator, with Programmer word count at 01C,and P light blinking.

3. Interactive Tests
   a. Press Stop
   b. Press Keyboard
   c. Load data 00 on word count 01C.
   d. Advance word count to)1D (Press FWD).
   e. Load Data 01.
   f. Press Program
   g. Press Execute
   h. After several seconds, observe PASS indicator with programmer word count at 01D and V lights blinking.

4. Duty Cycle Test
   a. Press Stop
   b. Press Keyboard
   c. Load Data 00 on word count 01D
   d. Advance word count to 01F (Press FWD)
   e. Load Data 01

f. Press Program
g. Press Execute
h. After several seconds, observe PASS indicator with Programmer word count at 01F and P light on.

This completes test procedures for MOS Digital Cards with interactive programming capabilities. If FAIL is indicated in any of the above tests, DO NOT use the Digital Card for PROM programming.

MOS INTERACTIVE PROGRAMMING TESTS FOR P5

Certain MOS Program Card Sets utilize interactive programming techniques. That is, pulse duty cycles are controlled by PROM temperature, and the re-program pulse train lengths are proportional to the number of pulses required to initially program particular PROM words.

Performance check of MOS interactive functions requires installation of the Digital Card into the Universal Calibrator. These tests, if required, are found at the bottom of the Calibration Chart under the heading "INTERACTIVE PROGRAMMING TESTS," and should be performed following Analog Card tests.

1. Turn programmer power OFF.
2. Unplug connector J1 at the Analog card; unplug connector J2 at the Universal Calibrator.
3. Remove Analog Card with attached 26-conductor cable and set aside.
4. Install calibrator into Digital Card slot.
5. Insert Digital Card (components forward) into Universal Calibrator top edge connector.
6. Connect 16-conductor cable to Digital Card J1 with cable red strip to J1, pin 1. (Other end of cable remains in Calibrator J1).
7. With Calibration Adaptors using 702-1073 Rev. "E" assemblies or later, install JP1 and JP2 in Position A.

Test Procedure: To test the interactive programming functions of the MOS Digital Card proceed as follows:

1. Initialization
   a. Turn Programmer power ON.
   b. Press: RESET
      MANUAL
      ROM 2 - ROM 2
      PROGRAM
      START
2. Abort Test
   a. Slew Programmer Word Count FWD to:

DEC	HEX	OCT
28	1C	034

   b. STOP
   c. START
   d. Load input Bit 1 (only)
   e. FWD (momentarily)
   f. After several seconds, observe PASS/FAIL indicator; if PASS is indicated Data A and Data B lights should be extinguished.
3. Interactive Tests
   a. STOP
   b. START
   c. FWD to Word Count

DEC	HEX	OCT
29	1D	035

   d. Load input Bit 1 (only)
   e. FWD (momentarily)
   f. Observe PASS/FAIL indicators, with Programmer Word Count at:

DEC	HEX	OCT
30	1E	36

4. Duty Cycle Test
   a. STOP
   b. START
   c. FWD to Word Count,

DEC	HEX	OCT
31	1F	037

   d. Load Bit 1 (only)
   e. FWD (momentarily)
   f. Observe PASS/FAIL.

This completes test procedures for certain MOS Digital Cards with interactive programming capabilities. If FAIL is indicated in any of the above tests, DO NOT use the Digital Card for PROM programming.

MOS INTERACTIVE PROGRAMMING TESTS

Certain MOS Program Card Sets utilize interactive programming techniques. That is, pulse duty cycles are controlled by pROM temperature, and the reprogram pulse train lengths are proportional to the number of pulses required to initially program particular pROM words.

Performance check of MOS interactive functions requires installation of the Digital Card into the Universal Calibrator. These tests, if required, are found at the bottom of the Calibration Chart under the heading, "INTERACTIVE PROGRAMMING TESTS," and should be performed following Analog Card tests.

1. Turn programmer power OFF.

2. Unplug connector J1 at the Analog card; unplug connector J2 at the Universal Calibrator.

3. Remove Analog Card with attached 24-conductor cable and set aside.

4. Move calibrator test fixture to digital slot. Insert digital card.

5. Connect 16-conductor cable to Digital Card J1 with cable red stripe to J1, pin 1. (Other end of cable remains in Calibrator J1.)

Test Procedure. To test the interactive programming functions of the MOS Digital Card proceed as follows:

1. Initialization

   a. Turn Programmer power ON.

   b. Press: RESET
      MANUAL
      ROM 2 - ROM 2
      PROGRAM
      START

2. Abort Test

   a. Slew Programmer Word Count FWD to:

DEC	HEX	OCT
28	1C	034

   b. STOP

   c. START

   d. Load input Bit 1 (only)

   e. FWD (momentarily)

   f. After several seconds, observe PASS/FAIL indicator; if PASS is indicated Data A and Data B lights should be extinguished.

3. Interactive Tests

   a. STOP

   b. START

   c. FWD to Word Count,

DEC	HEX	OCT
29	1D	035

   e. Load input Bit 1 (only)

   f. FWD (momentarily)

   g. Observe PASS/FAIL indicators, with Programmer Word Count at:

DEC	HEX	OCT
30	1E	36

4. Duty Cycle Test

   a. STOP

   b. START

   c. FWD to Word Count,

DEC	HEX	OCT
31	1F	037

   d. Load Bit 1 (only)

   e. FWD (momentarily)

   f. Observe PASS/FAIL.

This completes test procedures for certain MOS Digital Cards with interactive programming capabilities. If FAIL is indicated in any of the above tests, DO NOT use the Digital Card for pROM programming.

CIRCUIT DESCRIPTION

CIRCUIT DESCRIPTION, PROGRAM CARD SET

INTRODUCTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the PROM being programmed. Figure 4-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the PROM being programmed or read.

DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the PROM on the DO Bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command PROM program pulses from the analog card until either ABORT or REJECT is signaled, or until the bit is programmed.

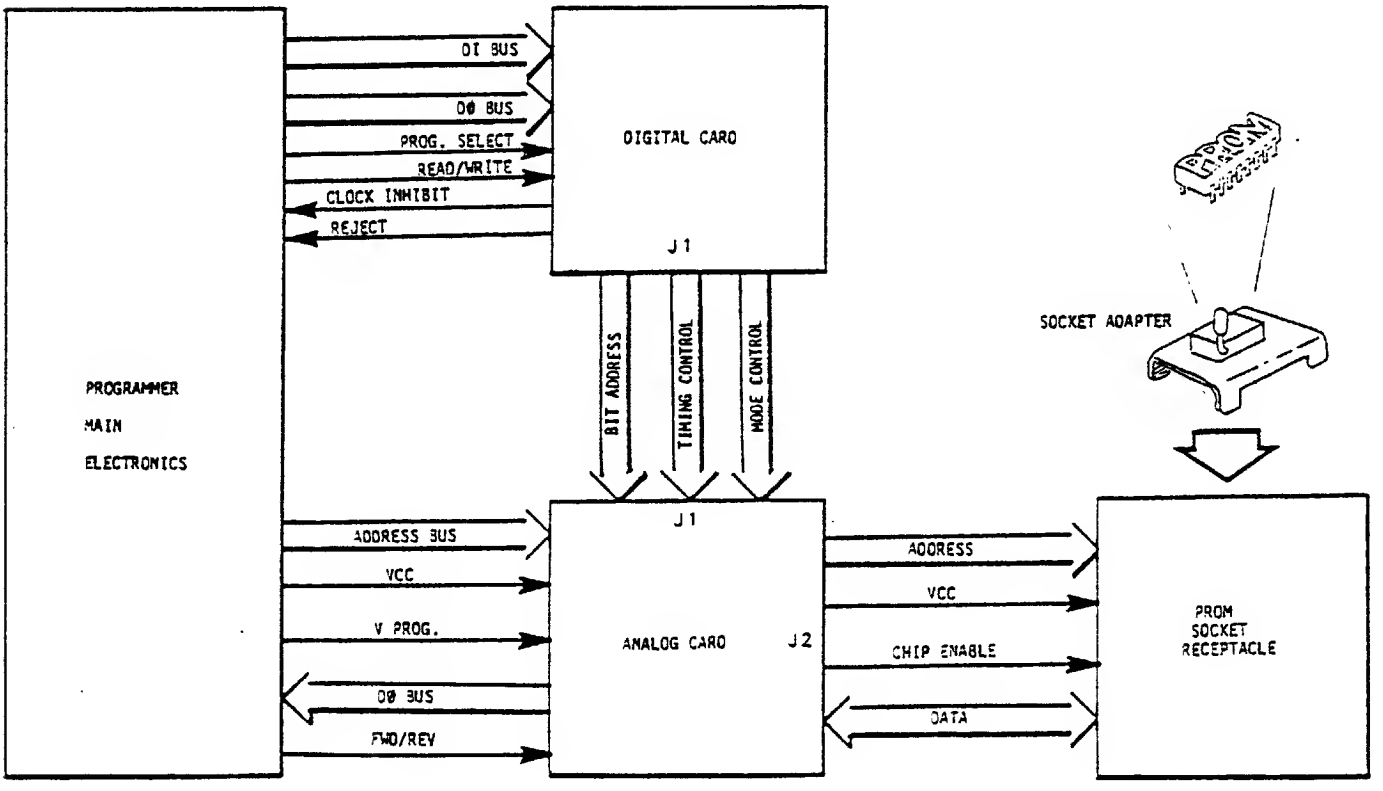
ANALOG CARD

The analog card receives bit addresses, word addresses, timing, and mode commands. Analog card output consists of PROM manufacturer's specified programming voltages and currents. When specified by the manufacturer, each programmed PROM bit is tested for loading and/or leakage. Following the program cycle, PROMs are read by the analog card to verify that programmed data matches truth table data.

DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow and timing. ROM truth tables, timing diagrams, jumper positions, and reject conditions are discussed. Detailed circuit schematics with timing diagrams and truth tables are found at the rear of this manual--refer to these for pin-out and interconnect information.

Fig. 4-1. Simplified Block Diagram of Program Card Set



MOS DIGITAL

GENERAL DESCRIPTION

The MOS Digital Card 701-1173 is a general purpose control system which is used in conjunction with Analog Cards of different configurations to program MOS PROMs.

The MOS Digital Card utilizes the technology of Intelligent Programming, Temperature Sensing and PROM based Jump Control System Logic. In order for the MOS Digital Card to properly perform with its associated Analog counterpart, an interface cable is connected over the top of the card from the J1 connector on the digital card to the associated connector on the analog card. This connector carries signals to the analog card for Programming, Verification, Selection, etc., and returns instructions for Temperature Interface Control.

Since the Logic system is based on PROM Interface Jump Control, changes in timing and interactive controls may be made in software without effecting the hardware configuration of the system.

INTELLIGENT PROGRAMMING

An intelligent programming scheme is used in the MOS digital card to provide an equation (x +Ax) of programming intelligence. This means that the device being programmed determines the level of normal program acceptance for verification of information, and the digital card keeps track of the number of program pulses or amount of energy that was required to attain the basic verification of data. At that time, an overprogram sequence is initiated which allows a fixed amount of energy to be programmed into the device at each word count to deeply program the data into the MOS memory cells. Following the overprogram sequence, normal digital verification occurs within the bus structure of the Programmer.

SELECTION AND CLOCK INHIBIT

Refer to the schematic diagram 008-1173. Input signals arrive on the Data Interface Bus on the left side of the drawing with Data Input and Output signals on the top of the drawing and the Interface connector to the analog card on the right side of the drawing labeled J1.

In order to select the instrument for programming, the Program (pin LL) must be in a Low condition, and the Write Inhibit Line (pin PP) must also be Low. As the Write Inhibit line is driven to a Low condition, and In Range Word Limit Control exists, Input Select Gate U15 Pin 1 becomes High. This line becoming high provides an enable to the Verify A and B lines enabling a ground on pin 19 and W on the external interface. The Input Select Gate also enables the Write Select Gate U8, which along with pin 9 becoming true, signals a Write condition. At Program time in the software, an instruction is issued on pin AA labeled Write, which is a low-going pulse. As this line becomes low, the output of the Write Select Gate U15 becomes high, which enables the Write Enable Gate U8. Prior to this, however, the stop line became high when the Start switch was pressed on the control panel. The Start condition allows the system to pass through a power-up cycle which enables the Power On Gate to release the Clear clamp on the Program Register U6. When clear is released, Clock timer U1 is also enabled due to NOR Gate U15 going low, allowing the Inverter U10 to become High thus turning on the Clock Timer U1.

The Timer Output provides a pulse into the clock input of the Program Register whose data inputs D1 through D4 arrive from PROM U7, signaling the next position to be addressed. The Program Register will be commanded to jump to any location that the PROM signals.

The start-up procedure allows power to be applied to the MOS Device, and the Logic PROMs command it to jump from 0 to 1 to 2 and then to 16. As the jump arrives at 16, the output of the logic PROM (pin 9) becomes low which causes a sector jump by enabling Pin E of U7 to high. The low condition also falsifies the Power ON Gate U8 so that the system returns to a clamp state with the Clock OFF and the Chip Enable on the Logic PROM (pin 15) Low.

JUMP CONTROL SYSTEM

The output of the Logic PROM on Pins 1, 2, 3, and 4 comprise a base-15 binary counter or jump sequence control whose outputs are presented to the input of the Program Register for D1, D2, D3, and D4. The Program Register is simply a D type register whose output follows the input at clock time. Therefore, as the input is told to move to a certain location, the output moves to that location at clock time, which then addresses the PROM for the next location desired at the next clock pulse. For this reason, complete flexibility of moving in one location to the other is programmed in the Logic PROM.

TIMING PROM

A second PROM (U5) follows the Logic PROM on its input address, and has eight output lines which are buffered and presented to the analog card. The Low pass filter networks at the input of the 7404 Buffers being applied to Connector J1 are to filter out spikes caused by changing addresses with the Chip Enable in an assert condition. The Timing PROM is programmed to desired functions to perform Power Control, Chip Enable, Temperature Tests or any other voltage or level controls desired. The timing diagram associated with the device under test determines what the program of this PROM shall be.

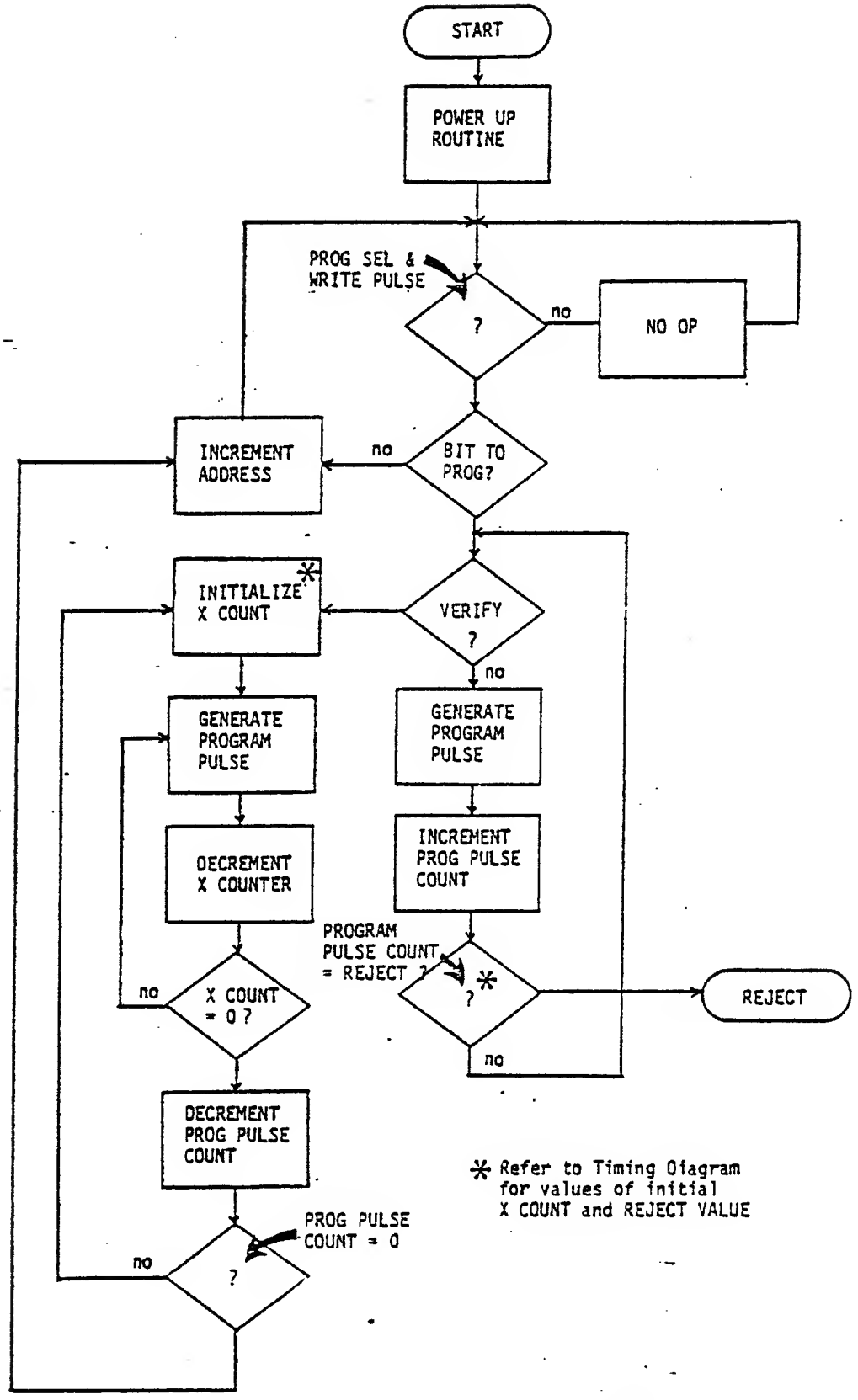


Figure 4-2. Flow Diagram of Program Cycle

CIRCUIT DESCRIPTION

TIMING DIAGRAM

Referring to the timing diagram 00711871, the upper section of the drawing shows the flow of program used with the MOS digital card. The instructions in the boxes are the Jump instructions which are used in the course of programming the PROM. Starting at Location 00, Start occurs for the Power UP cycle which causes a jump to 01, 02, and then to 16 which causes Stop. This cycle allows power to be applied to the system prior to a Write condition being executed.

As a Write instruction is issued, the Program is functioning in the loop 16 to 25 and upon reviewing the two PROM programs on the right hand side of the drawing, it can be seen on PROM U7 that the first four lines are used for program addresses, so that location 16 addresses location 17, and 17 addresses 18, etc., for a sequential count subroutine. This does not necessarily have to be sequential in order to properly function as the Jump Control system may cause a jump to any required location without interrupting the sequence. The instructions issued by the remaining four lines of PROM U7 are Test, Clock Rate, Temperature Test, and High/Low Order for control of PROM selection. Referring to the timing in the left side of the drawing, it can be seen that the High/Low Order line as controlled by U7 Pin 8, is executed after location 01. The test for temperature occurs at location 17 and the data test occurs at clock 19.

The second PROM U5 controls selection of other functions associated with the programming of the particular PROM. The associated lines VSS, VBB, Data Enable, Temperature Test, Program and Chip Enable, provide the timing associated with the Timing Diagram. As bits are programmed into the PROM, the particular functions desired are present so that Timing may be altered or adjusted as required.

PROGRAM COUNTER

Referring to the MOS Digital Logic Drawing 008-1173, the Test Pulse exiting the Logic PROM U7 is presented to a Count Enable Gate U11 as a low-going pulse. For a particular attempted program of the data into the PROM, a Test Pulse is issued prior to enabling Program, and slightly after the enable of the Chip Enable line for the PROM to test for Data Compare. The Input Data from the Control Card arriving on the DI Bus and the output of the PROM arriving on the DO Bus are exclusively or'd together by Gates U18 and U17. If a non-compare exists on any one of the eight lines, the wire or'd output line becomes low, thereby enabling the Count Enable Gate U11. The Test Pulse arriving from the PROM therefore exits U11 to create a Count Up Pulse applied to U13 Pin 5 of the Up/Down Program Counter.

As the program passes through one sequence of operation, the Program Counter is incremented by 1 and the Program X Count is loaded via Nor Gate U11 to the Preset Count of the Multiplier. The Program Sequence will continue to look until a verification occurs on the DO versus the DI Bus. This means that the basic count of the number of pulses required to program the PROM have been recorded in the Up/Down Program Counter. As soon as verification has occurred, the Test Pulse is applied through Inverter U9 Pin 11, delayed by the integrating network, and passes through Inverter U10 to cause a decrement of the Overprogram Count Multiplier U14. The Overprogram Counter Multiplier decrements one time for each Program Pulse in an overprogram Mode until a Borrow occurs exiting on U14 pin 13. The Borrow Pulse is applied to the downcount of the main Up/Down Counter U13 pin 4, and also through Inverter U10 pin 5, to cause a Preset or Loading of the Multiplier once again into the Program X Counter U14. Overprogramming continues in the PROM by the Multiplier times the Up/Down Program Counter, which accomplishes the programming formula $(x + Ax)$, until a Borrow Pulse is detected at U12 pin 13. This means that the Program Up/Down Counter has arrived at Count 0 and as that occurs, the low-going pulse at U12 pin 13 drives the Clock U1 OFF via Diode CR6, and falsifies the Gate U9 pin 5 thereby releasing the Clock Inhibit line pin Y on the instrument. The instrument is then released at that point to continue into a Digital Verify Mode and at that time AA (the the program awaiting the next Write command.

TEMPERATURE SENSING

A Pause/Temperature Sense network U1 is located in the lower right hand corner of the drawing. This device is a Level Comparator which has a selectable reference level adjusted by the 10 turn potentiometer R6, which provides a .25 V drop across Resistor R1 for reference. This potential is applied to Pin 2 of U2. If the VBB input line the output pin 7 goes to ground, thereby stopping the clock until the condition has corrected itself. Temperature Sensing occurs via a Diode network within the PROM which causes a difference in conduction characteristics as the temperature increases. This device, therefore, allows for Programming Control by temperature as well as overprogramming requirements, as determined in the PROM itself.

WORD LIMIT

Word Limit on this Card is accomplished by three jumpers at locations A8, A9, and A10. The Jumper selection JP2 is used so that as the particular lines becomes HIGH (as example A8 with Jumper JP2 in), the output of Inverter U20 Pin 12 becoming LOW passes through double Inverter U20 Pin 6 to exit on Pin CC to cause Word Limit selection on the Control Bus.

OUTPUT SELECTION

The Read Gate U8 is a 7400 device. U8 pin 3 when HIGH, selects the Analog Data Output Gates to present the data to the DO Bus. This Gate functions in two modes:

1) When Write Select is present, and Word Limit is within range, Gate U15 pin 1 is true or HIGH. If the Read Pulse is not at Pin X, that line being LOW allows U16 pin 6 to become HIGH therefore allowing the Write Output Enable Gate U8 pin 6 to become true or LOW, thereby addressing the Read Gate U8 pin 2.

2) READ MODE. If Read Inhibit is selected, Pin RR is ground, and if the Read Pulse is present, Pin X becomes HIGH thereby enabling the Read Output Select Gate U15 pin 4, which when inverted by U3 Pin 6 enables the Read Gate U8 pin 1.

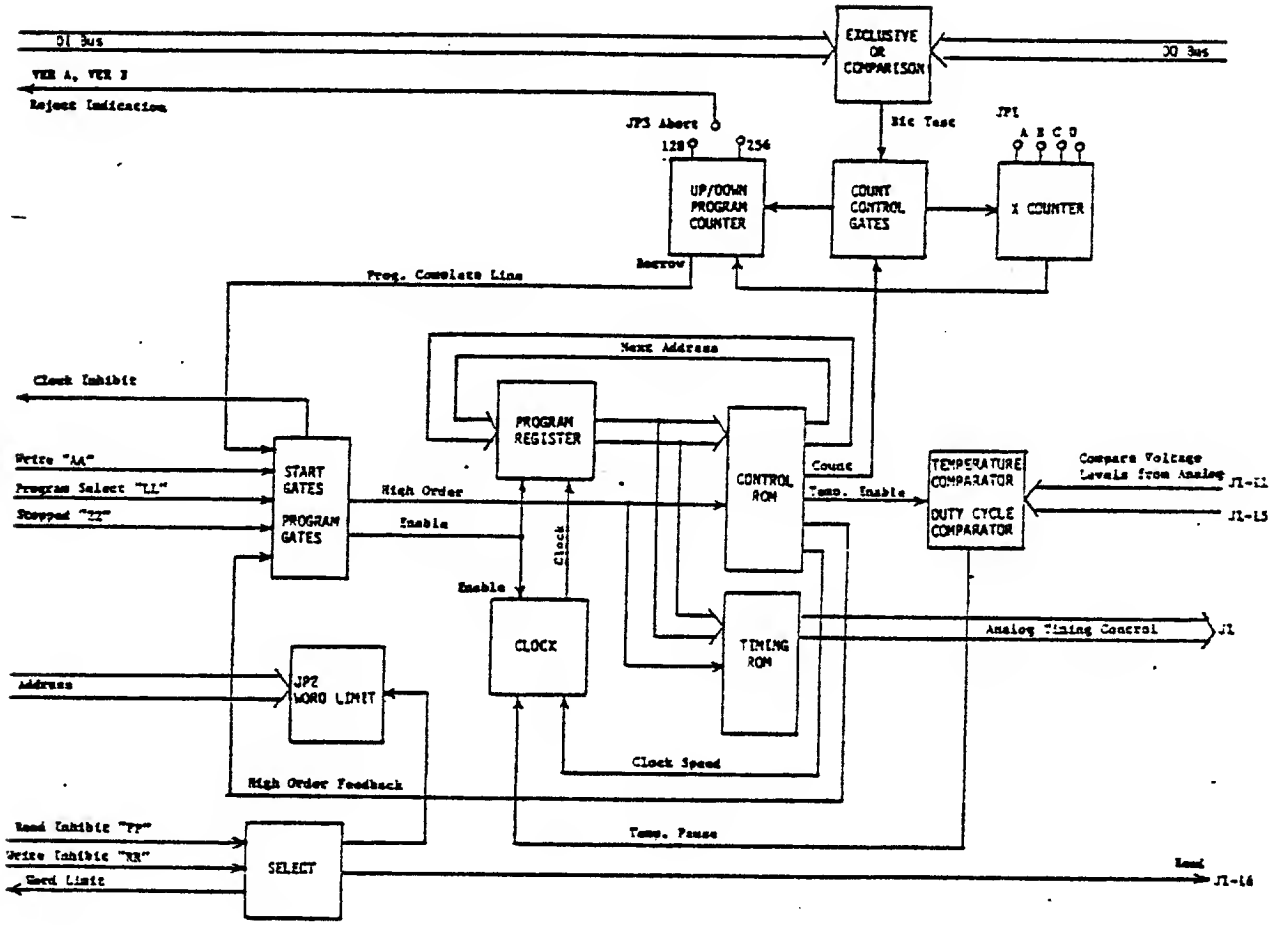


Figure 4-3. Block Diagram, 1173 Digital Program Card

CIRCUIT DESCRIPTION, 1183 ANALOG CARD

INTRODUCTION

The following paragraphs describe the electrical operation of the 1702/1702A Analog Card 701-1183, which is shown in block diagram form in figure 4-4. This card is used in conjunction with the MOS Digital Card to program and read 1702 and 1702A MOS 256x8 PROMs. The 1702 programmed logic level is VOH; the 1702A programmed logic level is VOL. Either device may be programmed or read simply by changing a jumper position on the 1183 Analog Card, as shown in Figure 4-2 and on page 1-2.

The Analog Card contains two connectors; one 16 pin, the other 26 pin. The MOS Digital Card provides control signals to the Analog Card through the 16 pin DIP connector J1. The PROM being programmed or read is connected through the 26 pin DIP connector to Analog Card electronics.

ADDRESS BUFFERS

Address Buffers accommodate the eight incoming address lines, AØ-A8, emanating from the Digital Card. The Buffers consist of exclusive OR gates U20-U21 followed by High Voltage Drivers U6, U8, U13, U15, U20, and U21. The OR gates allow the address data to be complemented by simply applying a high logic level to the common inputs. The High

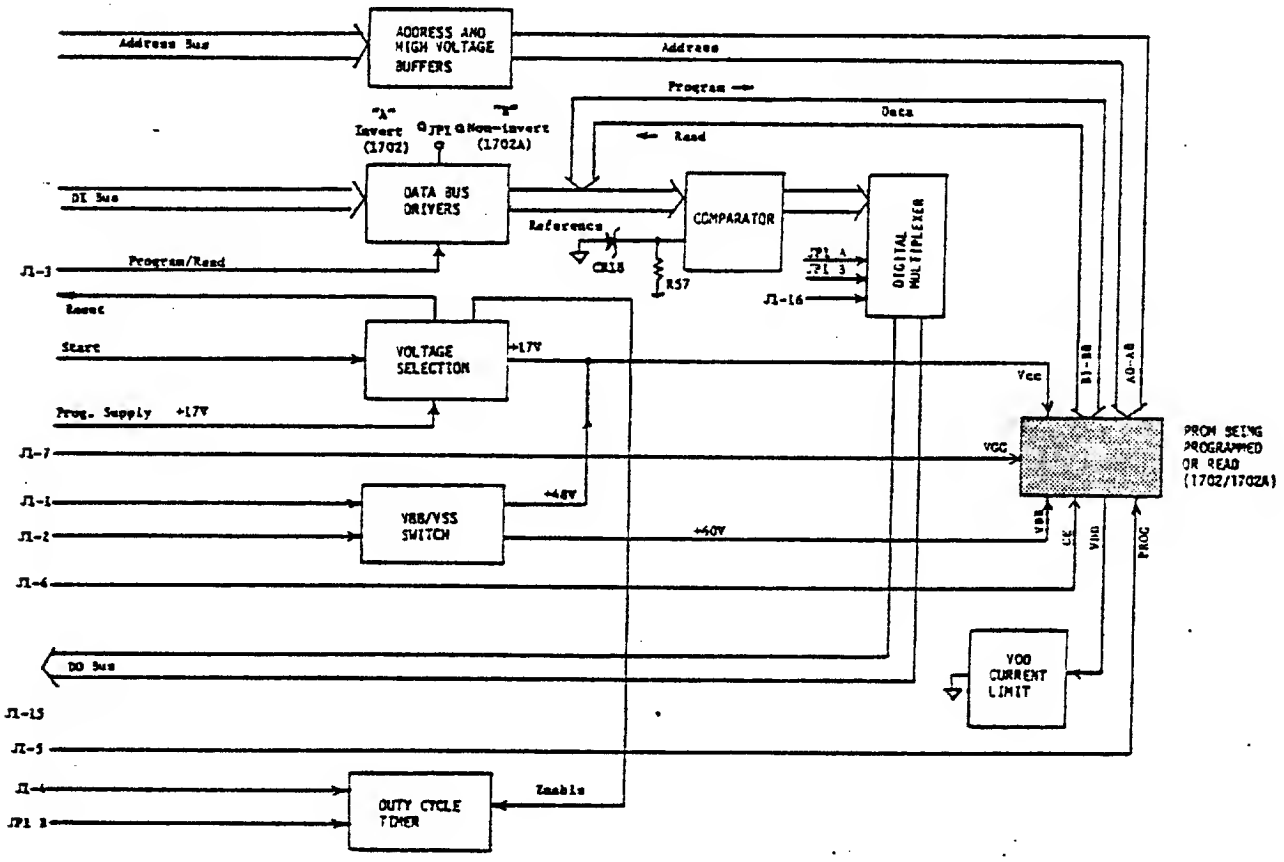


Figure 4-4. Block Diagram, 1183 Analog Program Card

Voltage Drivers with pullup resistors are used to provide the high voltages necessary when an address is asserted, or the low voltages necessary when an address is not asserted.

DATA PROGRAM BUFFERS AND DRIVERS

The Input Data bus (DI1-DI8) carries TTL data arriving from the Control Card of the Programmer. This data is presented to exclusive OR gates U18-U19. Jumper JP1 controls data inversion; in the A position (17D2 PROMs) incoming data is inverted, in the B position (1702 PROMs) data is not inverted. The following description assumes JP1 is in the A position.

The outputs of the OR gates drive gates U5, U7, U12, U14, which invert the data to a high or open state Bit to Program. Buffer outputs are applied directly to the 26 pin DIP connector on lines B1-B8; in addition, Buffer outputs are connected to the inputs of Comparator U10, U11. During PROGRAM, J1-3 goes high, and DI Bus data is tranferred to the PROM. During READ, J1-3 is low, the Buffers are disabled, and data from the PROM is presented to the Comparator.

DATA COMPARATOR

During READ, data lines from the PROM are presented to Comparator U10, U11. READ reference voltage at the negative comparator input is derived by CR18 and R57. The crossover from high to low determines the output level of the Comparator; READ reference is clamped at 3 volts below VSS. A LOW detected from the PROM causes comparator output to become low.

DIGITAL MULTIPLEXER

Comparator outputs are fed to Digital Multiplexer U16, U17, which can complement input data, not complement the data, or float its outputs. The outputs float if J1-16 is low. If J1-16 is high and if J1 is in position B, the input data will be complemented (17D2A PROMs); a high (programmed 1702A bit) will cause a low on the DO Bus. If J1 is in position A, a low (programmed 17D2 bit) will cause a low on the DO Bus. Data on the DO Bus is used for comparison on the MOS Digital Card, and for further verification on the Control Card.

VOLTAGE SELECTION

Voltage is applied to the PROM only after START goes high. High start voltage is inverted by U9 (see schematic) which turns on tranistor Q3. This allows +17 volt output from the programmable power supply to reach the PROM through current limiting resistor R12 and diode CR6. If excessive current is drawn by the +17V line, the voltage drop across R12 becomes excessive (0.5V or above), and transistor Q2 turns on. This supplies base current to Q8, which saturates and causes a RESET on line DD.

VBB-VSS SWITCH

J1-1 and J1-2 provide control to the VSS and VBB switch circuitry, Q4-Q7. When J1-1 goes high, it is inverted in U1, causing Q4 to saturate, hence connecting +48 volts to the VCC line. Operation is similar with J1-2, which connects the VBB line to +60 volts. These switches operate in PROGRAM only, overriding the +17 volt line from the voltage selection network. The +48 and +60 volt supplies are applied through current limit resistors R33 and R38. Diode CR5 is cut off by the +60 volt potential applied to VBB. If excessive current is drawn on either of these lines the voltage drop allows conduction from the positive source through R39 or R35, which turn on Q8 and drive the RESET line DD to low.

DUTY CYCLE TIMER

The temperature control circuitry of the MOS Digital Card is used in conjunction with the timer Q9, C11, R71 and U2 on the Analog Card to achieve the 2% duty cycle required to program the 1702 PROM. When JP1 is in the A (1702) position, gate U2 is enabled. A pulse arrives on J1 pin 4 to turn on transistor Q9 to charge C11. The voltage on C11 is monitored by the temperature test comparator on the Digital Card. Two clock pulses later, the Temperature Test Comparator is strobed on the Digital Card. Since the voltage on C11 is still high the Digital Card will pause. The pause will continue until the voltage on C11 drops to a level selected on the Digital Card, and the clock will step through the remaining portion of the program at the normal rate. If JP1 is in the B (1702A) position, U2 is disabled and the duty cycle is determined by the Digital Card.

VDD CURRENT LIMIT

The Transistor Q1 is used for current limiting on the VDD line. Two diodes CR7 and CR8 provide a standoff bias characteristic for the Transistor Q1 so that if excessvie current is driven through R23, Q1 is current limited for short circuit protection by the standoff bias and shutoff characteristic of the transistor.

REVERSE DEVICE TEST

The PROM Device 17D2 or 17D2A has a characteristic that allows detection of a Reverse condition by the instrument going into a current limit state, which shuts down or prevents START from occurring.

Warranty

Data I/O equipment is guaranteed against defects in materials and workmanship. The warranty period is ninety days on new equipment, and thirty days on used equipment. Warranty period begins on receipt of equipment. Data I/O will repair or replace, at Data I/O's option, any equipment found to be defective within the warranty period.

Warranty service will be provided by Data I/O within a reasonable amount of time after notification by the purchaser to Data I/O of equipment malfunction. This service shall not apply to equipment that has been subjected to abuse, misuse, negligence or accident as determined by Data I/O, or to which any modifications, alterations, or attachments have been made without written authorization from Data I/O, nor shall it apply if the equipment is installed or operated in an environment containing excessive dirt, dust, moisture, fumes, humidity, or extremes of temperature.

This warranty policy is in lieu of all other warranties, expressed or implied, unless standard warranty exceptions are granted by Data I/O in writing.

Service

After expiration of the warranty period, service and repairs are billed at standard hourly rates, plus expenses, portal-to-portal. Time and one-half rate will apply outside of normal working hours.

Cost of engineering (where applicable) and parts, plus the cost of installation is billed at standard service labor rates when implementing approved, customer requested modifications.

Shipment

Products returned to Data I/O should be accompanied by a letter or enclosure explaining the reason for their return and action requested of Data I/O. Please include the following additional information: Company name and address; attention of; method of shipment desired; serial number; date of purchase; billing information, and purchase order number.

All products returned to Data I/O must be sent prepaid F.O.B. The warranty is voided if returned items are not packaged by the customer in original packing material, or in other Data I/O approved containers. If reshipment method is not specified by customer, Data I/O will return products by most expedient shipping method, F.O.B. our plant.

Ship returned equipment to:

DATA I/O CORPORATION
1297 N.W. Mall
Issaquah, Washington 98027

From Europe:

DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

Parts Ordering

Orders for parts should contain the following information:

a. Description of part(s) and Data I/O part number(s).
b. Quantity of each item to be ordered.
c. Equipment serial number and model number.
d. Corporate name of firm.
e. Shipping address of firm, including zip code.
f. Full name of person ordering the part(s).
g. To whose attention the part(s) are to be shipped.
h. Billing information.
i. Purchase order number.
j. Method of shipment.

Please send all parts orders to:

DATA I/O CORPORATION
P O Box 308
Issaquah, Washington 98027

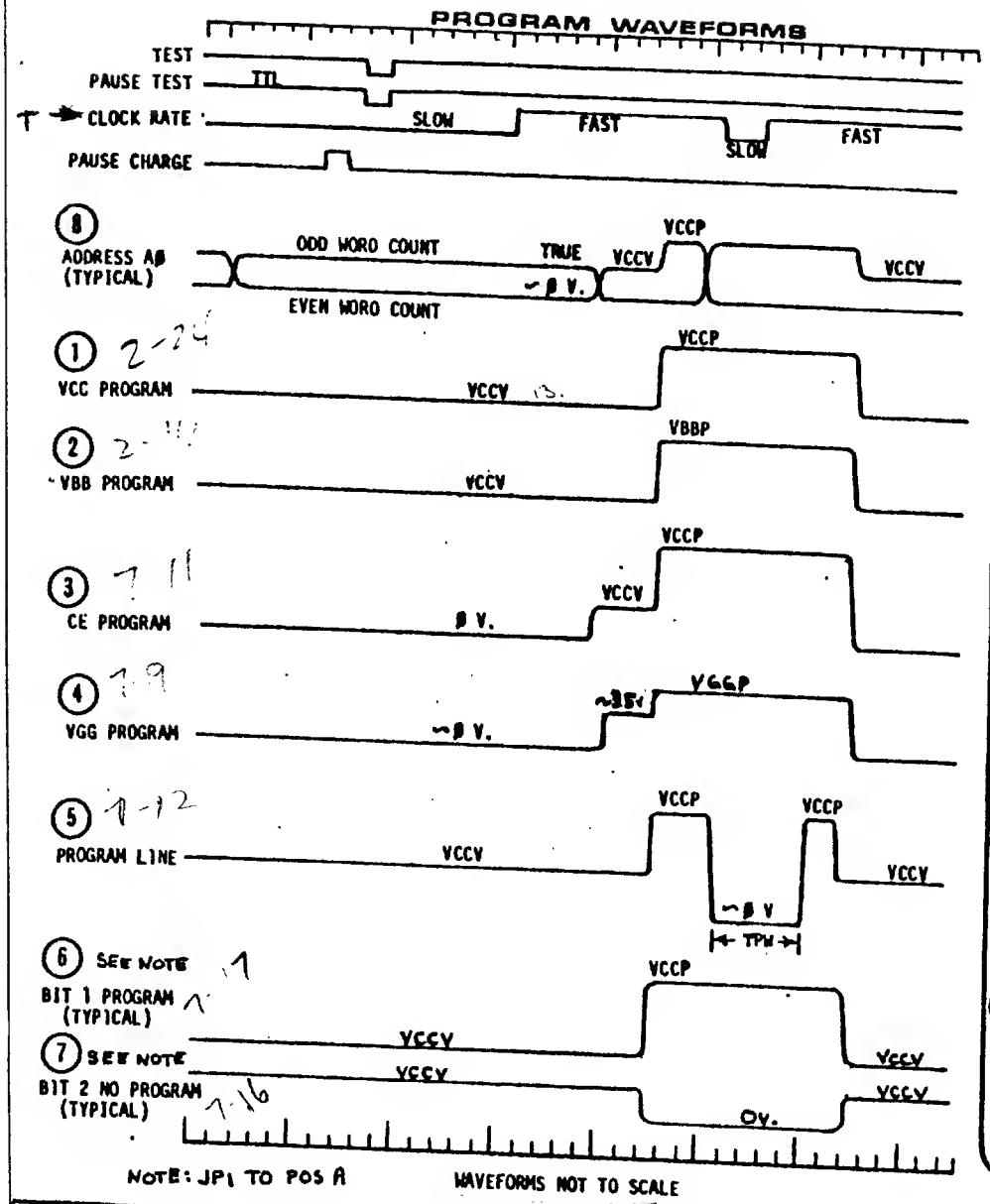
From Europe:

DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

1-79 CH #2594

FS 1	7-75	A	RELEASE
10	7-75	B	CH #339
2	7-76	C	CH #515
	7-77	—	ECR 1576
	7-77	—	ECR 2036

PROGRAM WAVEFORMS



NOTE: JP1 TO POS A WAVEFORMS NOT TO SCALE

NOTES

1173 DIGITAL JUMPERS

JP1	A, B, D	SHORT	A=4
JP1	C	OPEN	
JP2	256 (Word Limit)		
JP3	A	SHORT	Reject at 256
JP3	B	OPEN	

1183 ANALOG CARD JUMPERS

JP1 B=1702A = 20% Duty
JP1 A=1702 = 2% Duty

WAVEFORM VARIABLES

VCCP = + 47.0 TO +49.0 VOLTS
VCCV = + 13.3 TO +14.7 VOLTS
VGGP = +6.0 TO +13.0 VOLTS
VBBP = 60 ± 1.5 VOLTS
TPW = 2.0 ± 0.1 MSEC

ABORT IS SET AT 256 PULSES

1702A TIME ON APPROX. 3 SEC
1702 TIME ON APPROX. 30SEC

INTELLIGENT PROGRAMMING EQUATION:

N = X + A(X+1) -1
N = TOTAL NUMBER PULSES
A = MULTIPLIER = 4
X ≤ 256

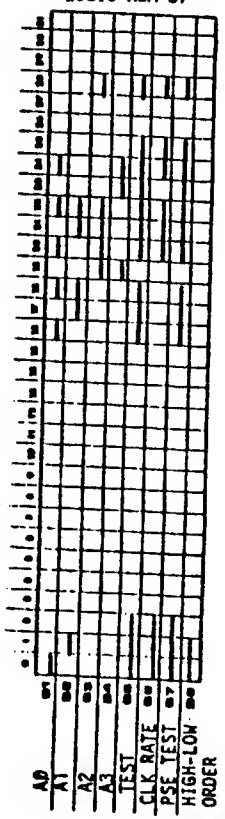
CARD SET POLARITY IS JUMPER-SELECTABLE (JP1 ON THE ANALOG CARD). FOR CALIBRATION, GROUND DIGITAL CARD J1 PIN 16.

(○) These waveforms correspond to call-outs on Calibration Chart 017-1183-1. Switch S2 and S3 of Universal Calibrator to indicated positions to obtain waveforms. Refer to dynamic test instructions in performance check section for detailed instructions.

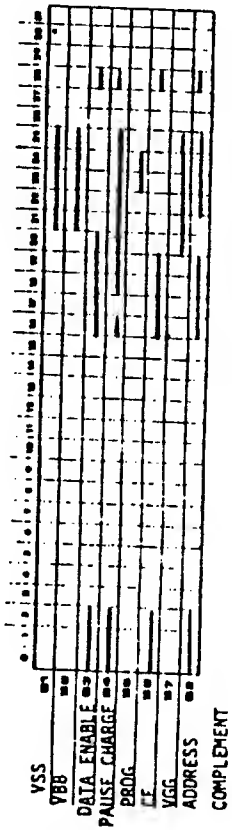
TRUTH TABLES

LINE : HI(1); NO LINE : LOW(0)

LOGIC ROM U7



TIMING ROM U5



DATA I/O REDMOND, WASH.

DRAWN BY MO
APPROVED BY

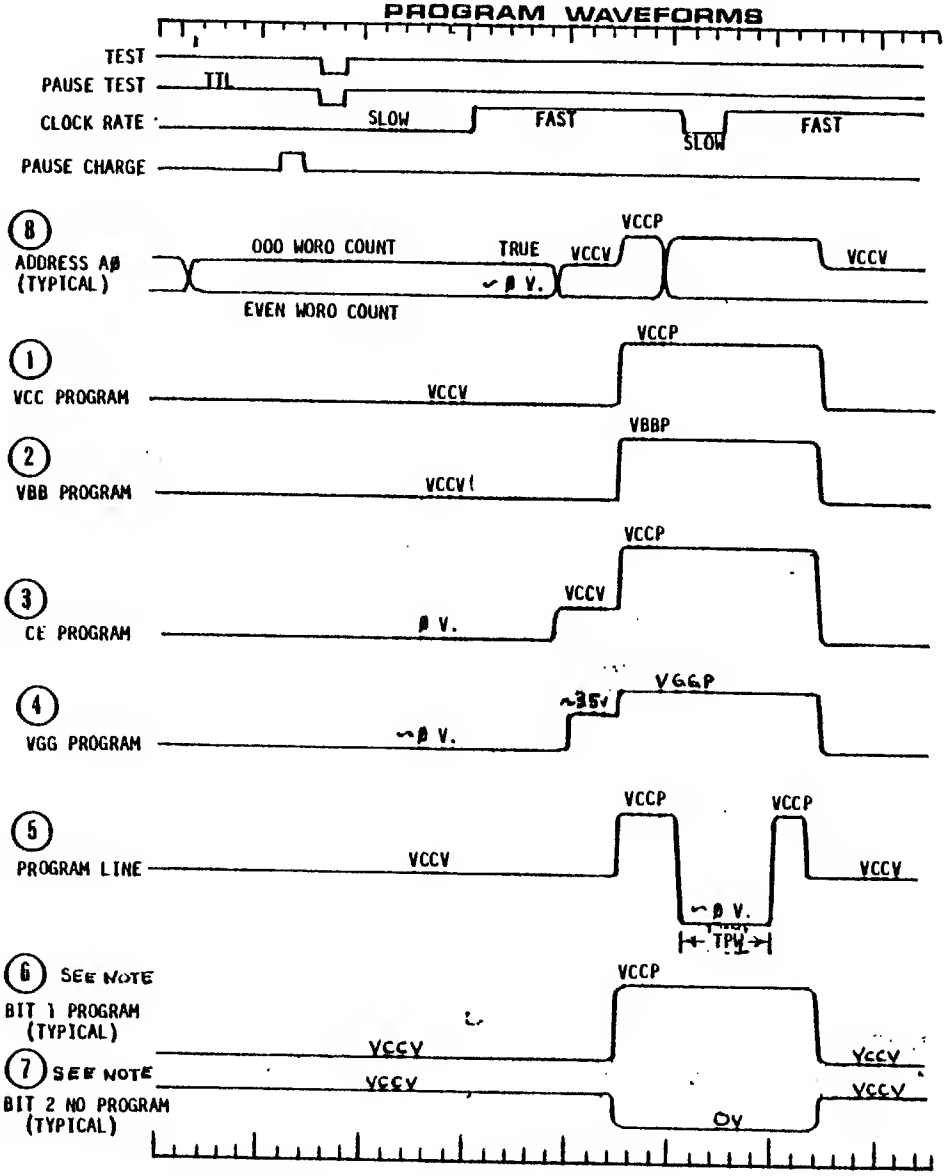
TITLE: 1702/1702A TIMING DIAGRAM

DATE: 6/24/76
DRAWING NUMBER: 007-1183-1

FOR REFERENCE ONLY

OBSOLETE

PROGRAM WAVEFORMS



NOTE: JP1 TO POS B. WAVEFORMS NOT TO SCALE

NOTES

1173 DIGITAL JUMPERS

JP1	A, B, D	SHORT	A=4
JP1	C	OPEN	A=4
JP2	256 (Word Limit)		
JP3	A	SHORT	Reject at 256
JP3	B	OPEN	Reject at 256

1183 ANALOG CARD JUMPERS

JP1 B=1702A = 20% Duty
JP1 A=1702 = 2% Duty

WAVEFORM VARIABLES

VCCP = + 47.0 TO +49.0 VOLTS
VCCV = + 13.3 TO +14.7 VOLTS
VGGP = +6.0 TO +13.0 VOLTS
VBBP = 60 ± 1.5 VOLTS
TPW = 2.0 ± 0.1 MSEC

ABORT IS SET AT 256 PULSES

1702A TIME ON APPROX. 3 SEC
1702 TIME ON APPROX. 30SEC

INTELLIGENT PROGRAMMING EQUATION:

N = X + A(X+1) -1
N = TOTAL NUMBER PULSES
A = MULTIPLIER = 4
X ≤ 256

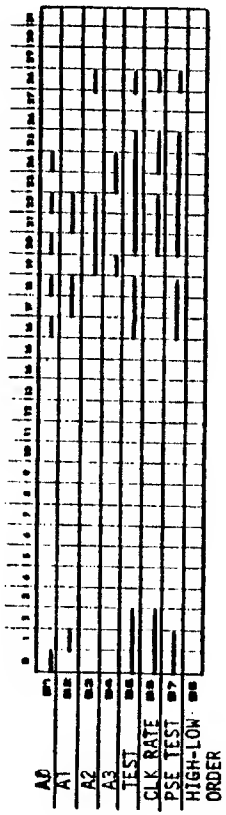
These waveforms correspond to call-outs on Calibration Chart 017-1183-1. Switch S2 and S3 of Universal Calibrator to indicated positions to obtain waveforms. Refer to dynamic test instructions in performance check section for detailed instructions.

	DATE	DM	REVISION RECORD	DR.
1	75	A	RELEASE	
10	75	B	CN #339	
2	76	C	CN #515	VD
7-77	—		ECR 1576	KJ
3-11	—		ECR 2076	KJ

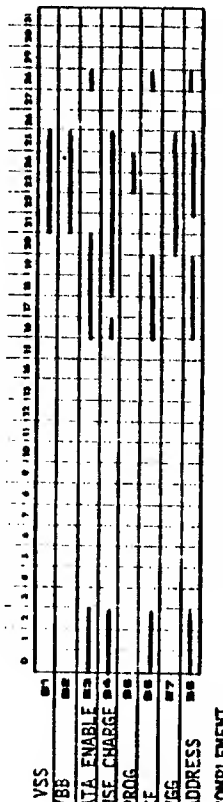
TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)

LOGIC ROM U7



TIMING ROM U5



DATA I/O ISSAQUAH, WASH.

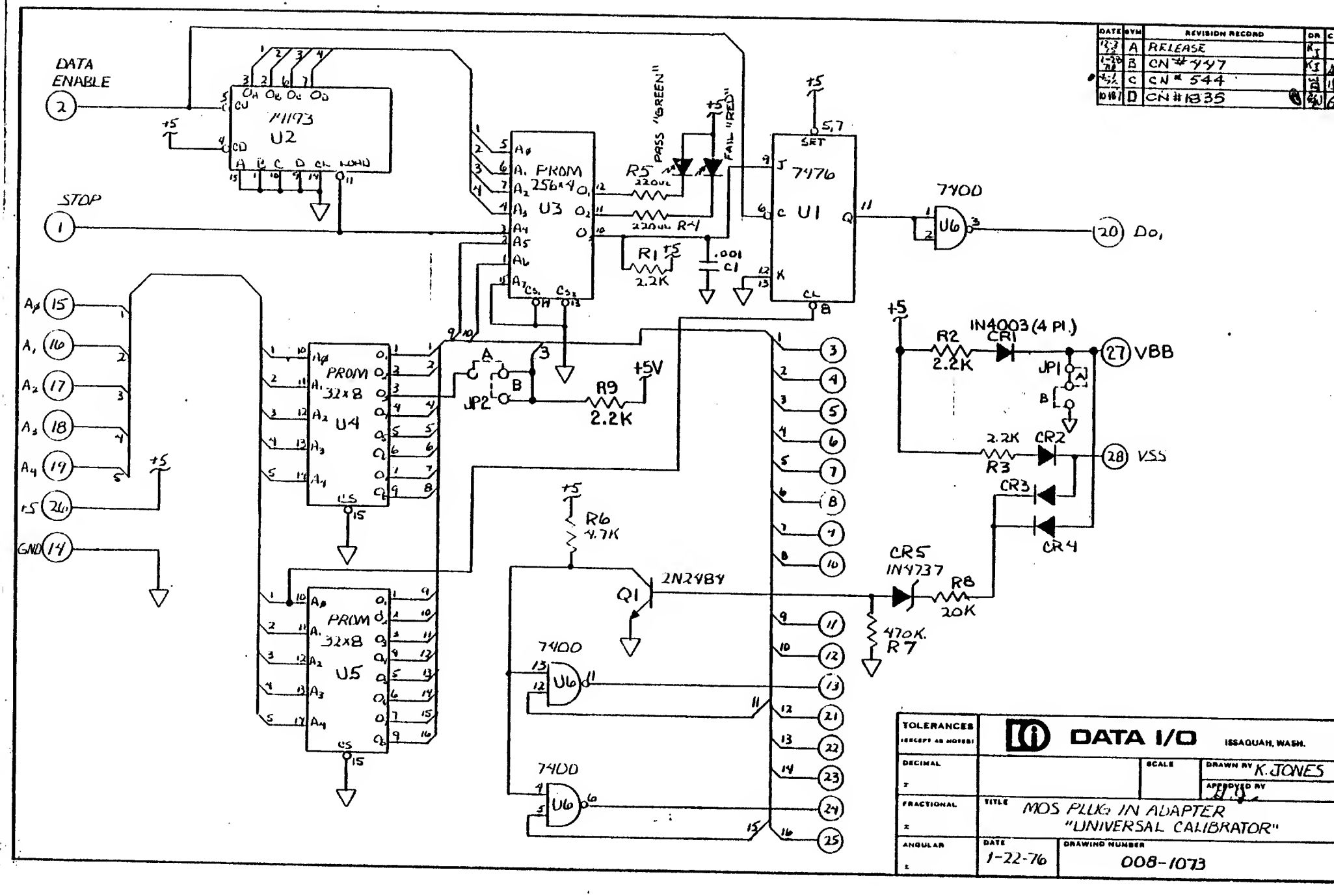
DRAWN BY LLO
APPROVED BY

TITLE
1702/1702A TIMING DIAGRAM

DATE 6/21/76

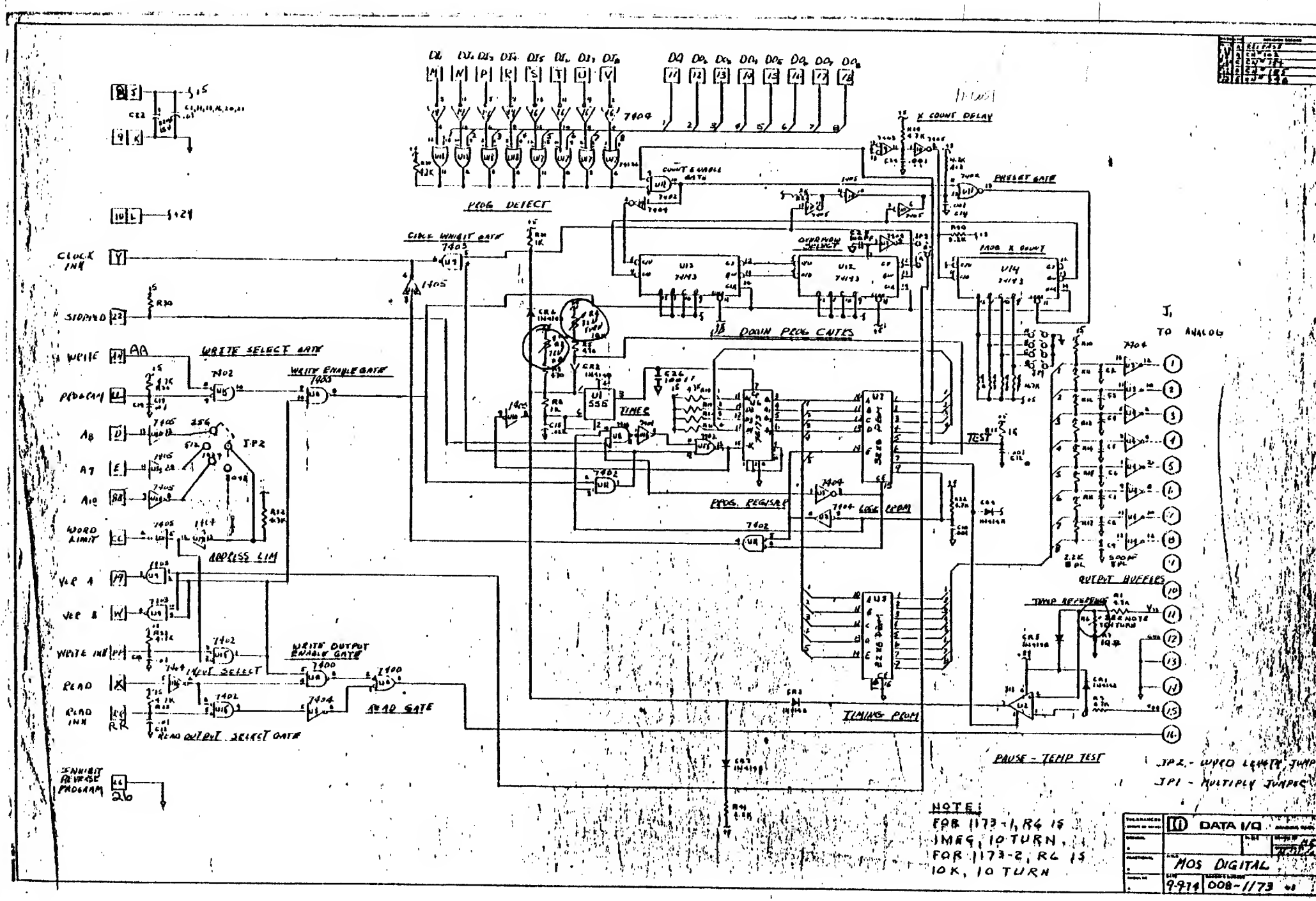
DRAWING NUMBER 007-1183-1

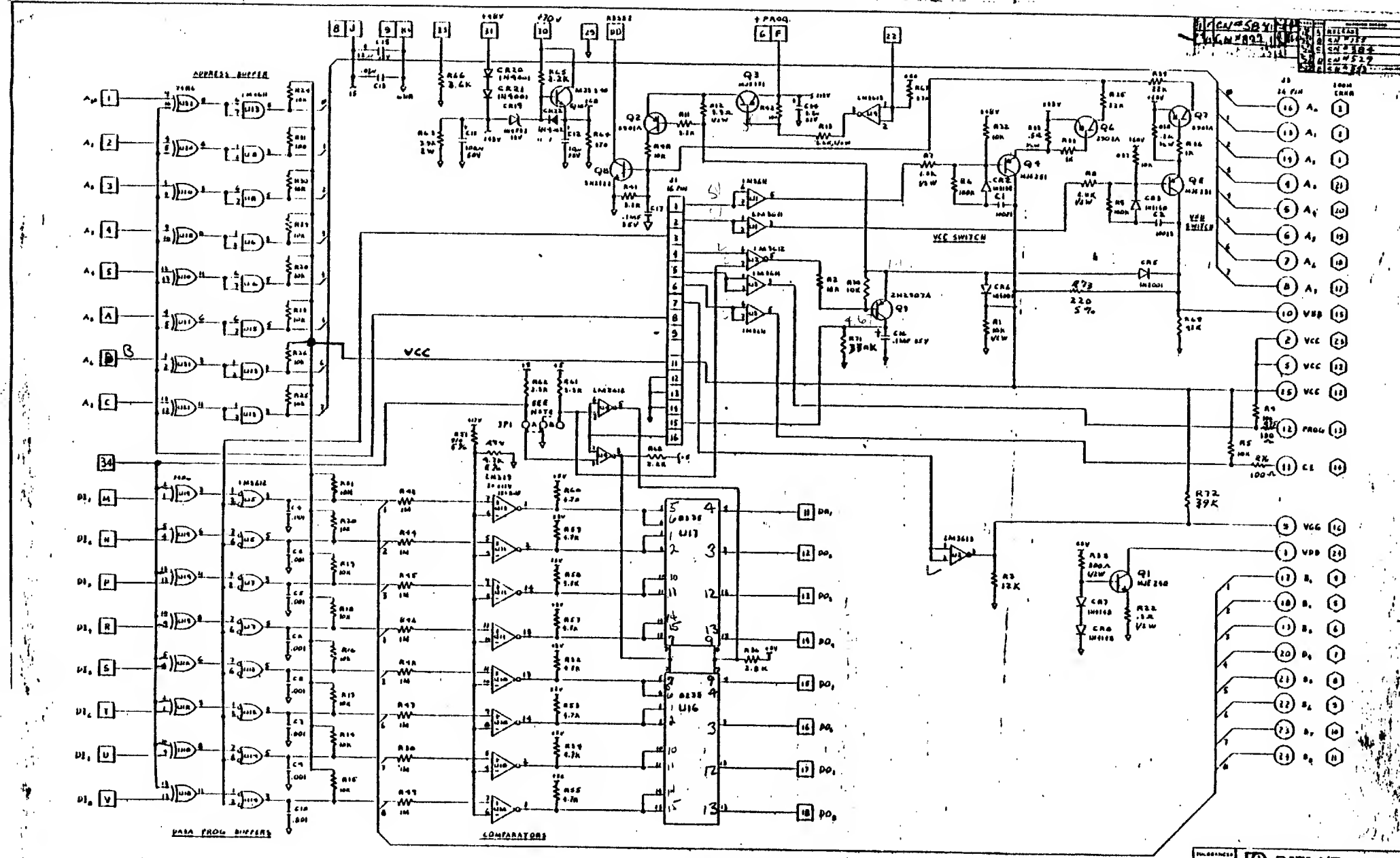
OBSOLETE

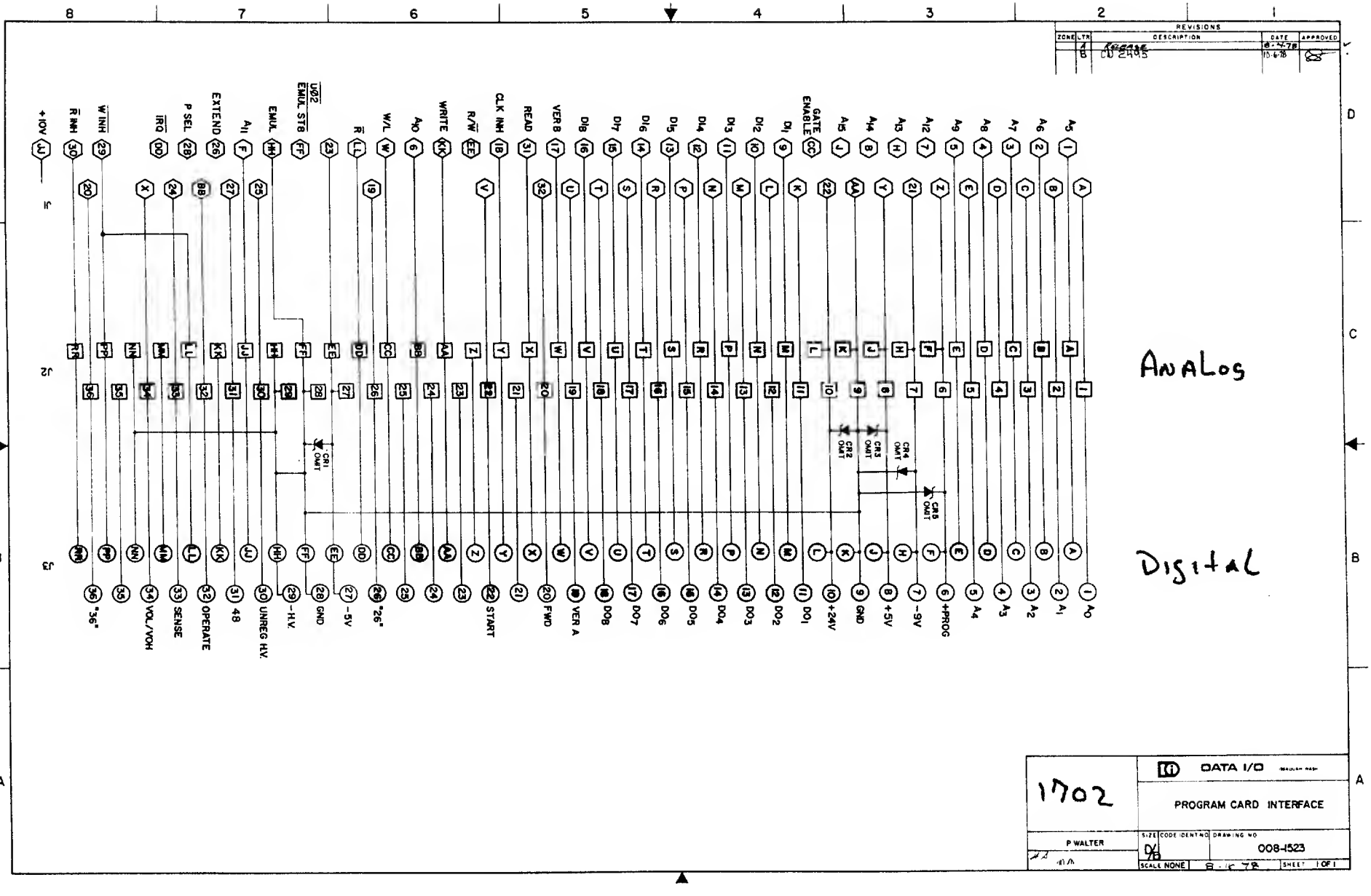


DATE	BYN	REVISION RECORD	DR
12-3-75	A	RELEASE	KJ
1-28-76	B	CN #447	KJ
4-1-76	C	CN # 544	KJ
10-18-76	D	CN #1835	KJ

TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL ±		SCALE	DRAWN BY K. JONES
FRACTIONAL ±	TITLE MOS PLUG IN ADAPTER "UNIVERSAL CALIBRATOR"		APPROVED BY
ANGULAR ±	DATE 1-22-76	DRAWING NUMBER 008-1073	


DI DI1 DI2 DI3 DI4 DI5 DI6 DI7
DO DO1 DO2 DO3 DO4 DO5 DO6 DO7
7404
X COUNT DELAY
PRESET GATE
PROG DETECT
CLOCK INH
CIRCUIT INHIBIT GATE
7405
OSCILLATION SELECT
PROG X COUNT
U13 74193
U12 74193
U14 74193
DOWN PROG GATES
SIGNED
WRITE
PROGRAM
WRITE SELECT GATE
WRITE ENABLE GATE
7402
7400
A8
A9
A10
256
512
TP2
U1 556
TIMER
PROG. REGISTER
LOGIC PROM
TEST
WORD LIMIT
ADDRESS LIM
VER A
VER B
WRITE INH
READ
READ INH
INPUT SELECT
WRITE OUTPUT ENABLE GATE
READ GATE
READ OUTPUT SELECT GATE
INHIBIT REVERSE PROGRAM
TIMING PROM
OUTPUT BUFFERS
TEMP REFERENCE
TO ANALOG
PAUSE - TEMP TEST
JP2 - WORD LENGTH JUMP
JP1 - MULTIPLY JUMPER
NOTE:
FOR 1173-1, R4 IS
1MEG, 10 TURN.
FOR 1173-2, R4 IS
10K, 10 TURN
DATA I/O
MOS DIGITAL
9-714
008-1173


ADDRESS BUFFER
DATA PROG BUFFERS
COMPARATORS
VCC SWITCH
VCC
PROG
NOTES
1. JP1 B TO 20%
2. JP1 A TO 2%
DATA I/O
INTEL 1702/1702A ANALOG
1-9-15
008-1183


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A Release 6-4-78
B ECO 2405 10-6-78
ANALOG
DIGITAL
A5 A4 A3 A2 A1 A0
+PROG -9V +5V GND +24V
D0 1 D0 2 D0 3 D0 4 D0 5 D0 6 D0 7 D0 8
VER A FWD START
-H.V. UNREG H.V. 48 OPERATE SENSE VOL/VOH -5V "26" GND
"36"
+10V
W INH R INH P SEL IRQ EXTEND A11 EMUL U92 EMUL STB R W/L A0 WRITE R/W CLK INH READ VER B D18 D17 D16 D15 D14 D13 D12 D11 GATE ENABLE A15 A14 A13 A12 A9 A8 A7 A6
CR1 OMIT CR2 OMIT CR3 OMIT CR4 OMIT CR5 OMIT
1702
DATA I/O
PROGRAM CARD INTERFACE
P WALTER
SIZE D/A
CODE IDENT NO
DRAWING NO 008-1523
SCALE NONE
8-1-78
SHEET 1 OF 1